Spartan-6 LX9 MicroBoard	
Avnet Design Services	
www.em.avnet.com/s6microboard	
Function	**Sheet Number**
Lead Sheet	1
Block Diagram	2
Architecture	3
FPGA Bank 0	4
FPGA Bank 1	5
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Spartan-6 LX9 MicroBoard Rev B
1/28/2011
9:47:02 AM

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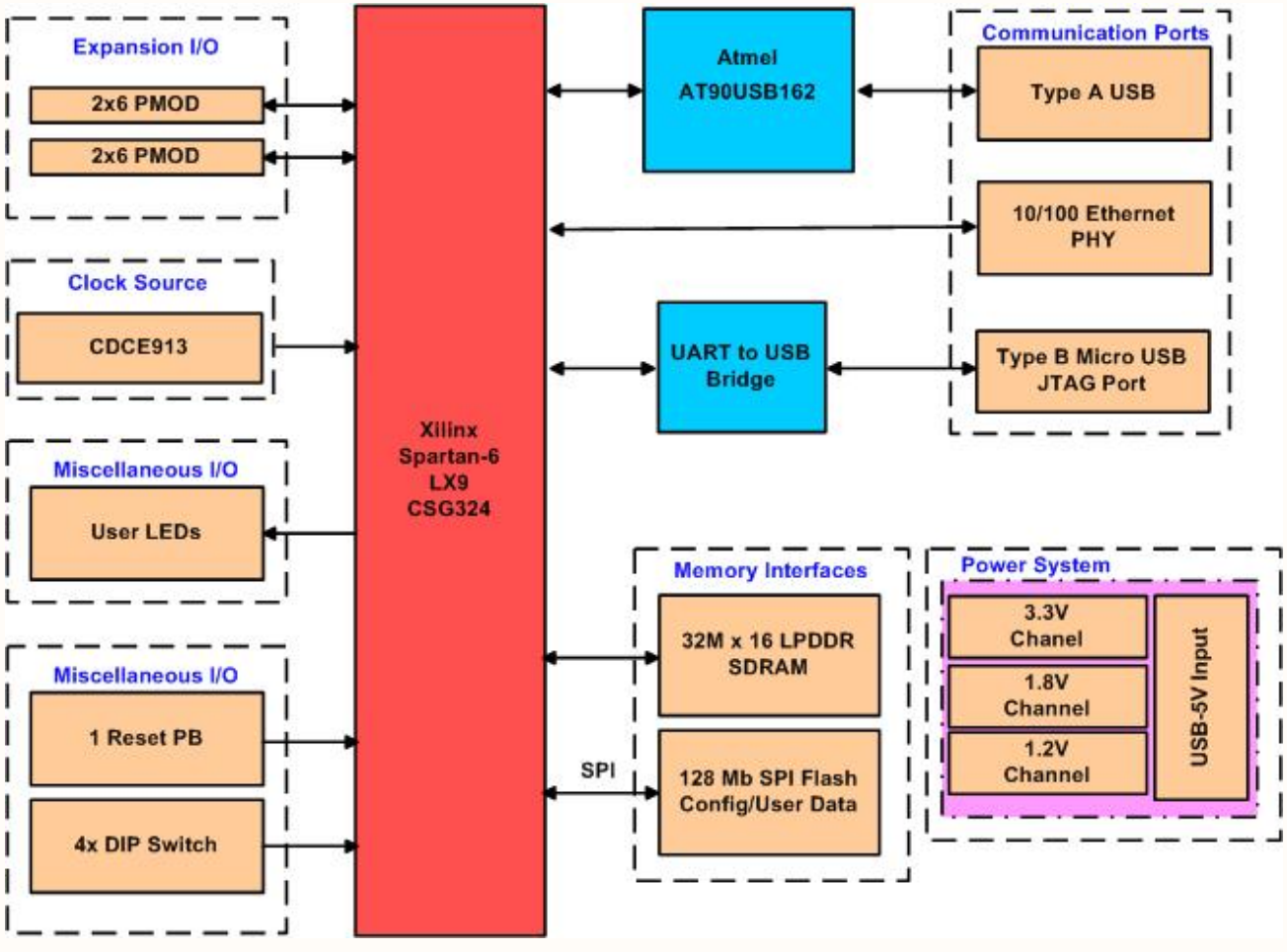
Avnet Engineering Services		
Title: Sheet 1 - Lead Sheet		
Size: B	Document Number: S6-LX9-SCH-B	Rev: B
Date: 1/28/2011	Sheet 1 of 10	



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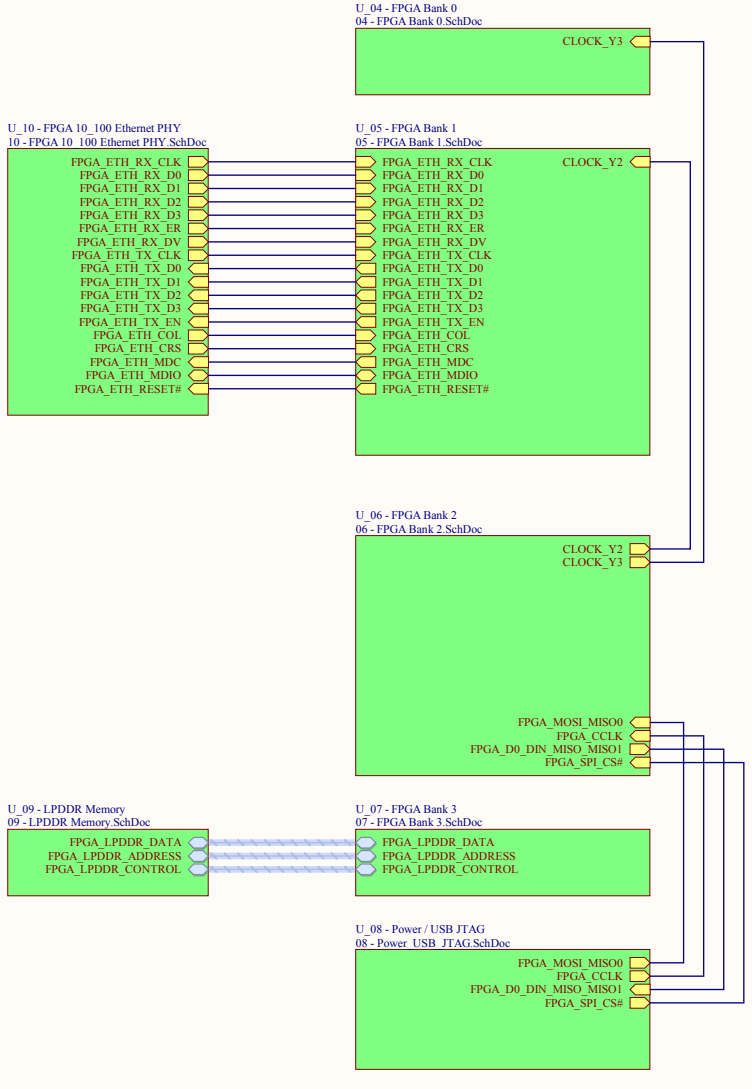
Avnet Engineering Services		
Title: Sheet 2 - Block Diagram		
Size: B	Document Number: S6-LX9-SCH-B	Rev: B
Date: 1/28/2011	Sheet 2 of 10	



MTG2
MOUNTING HOLE 125mil

MTG3
MOUNTING HOLE 125mil

MTG1
MOUNTING HOLE 125mil

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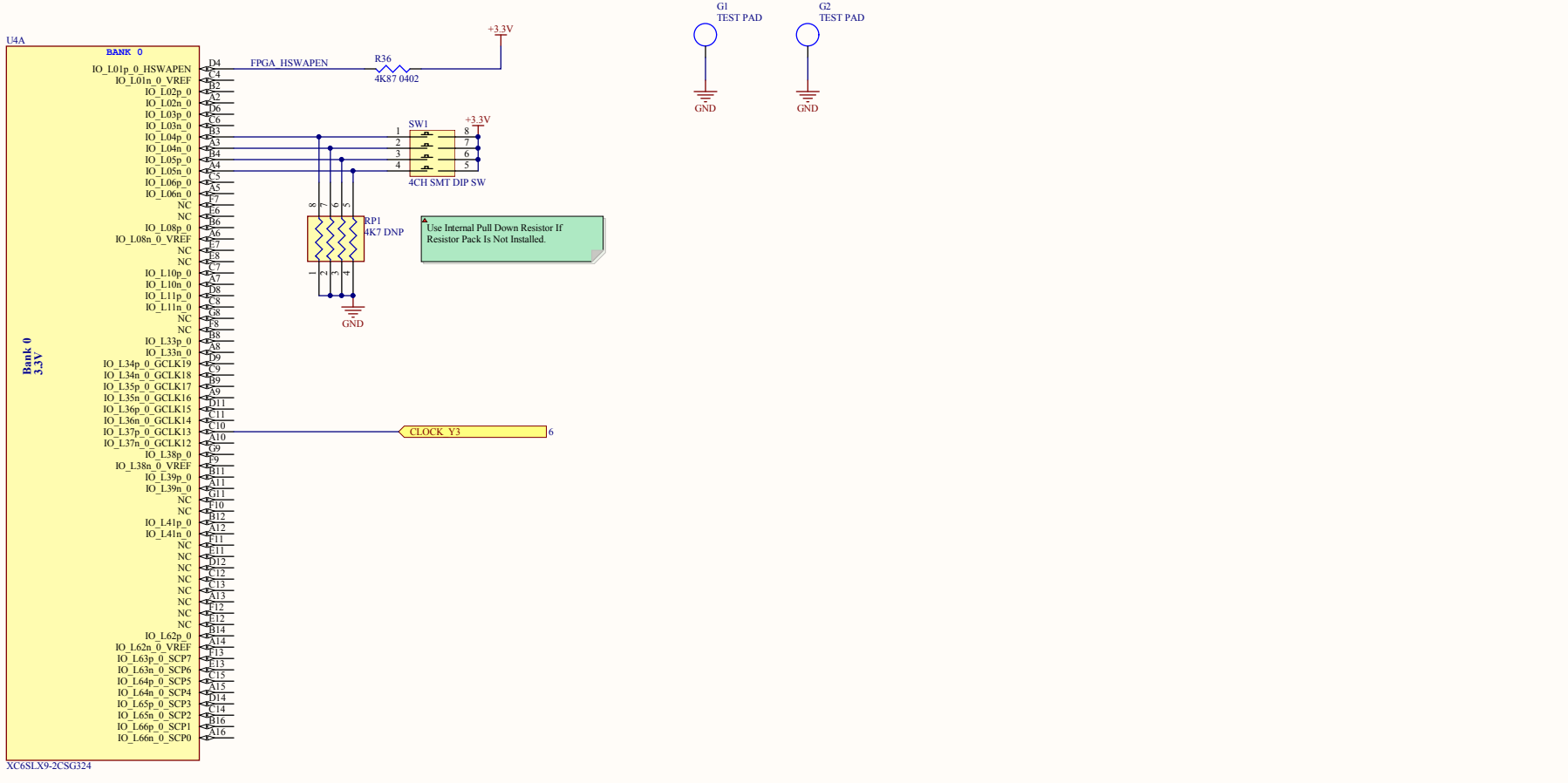
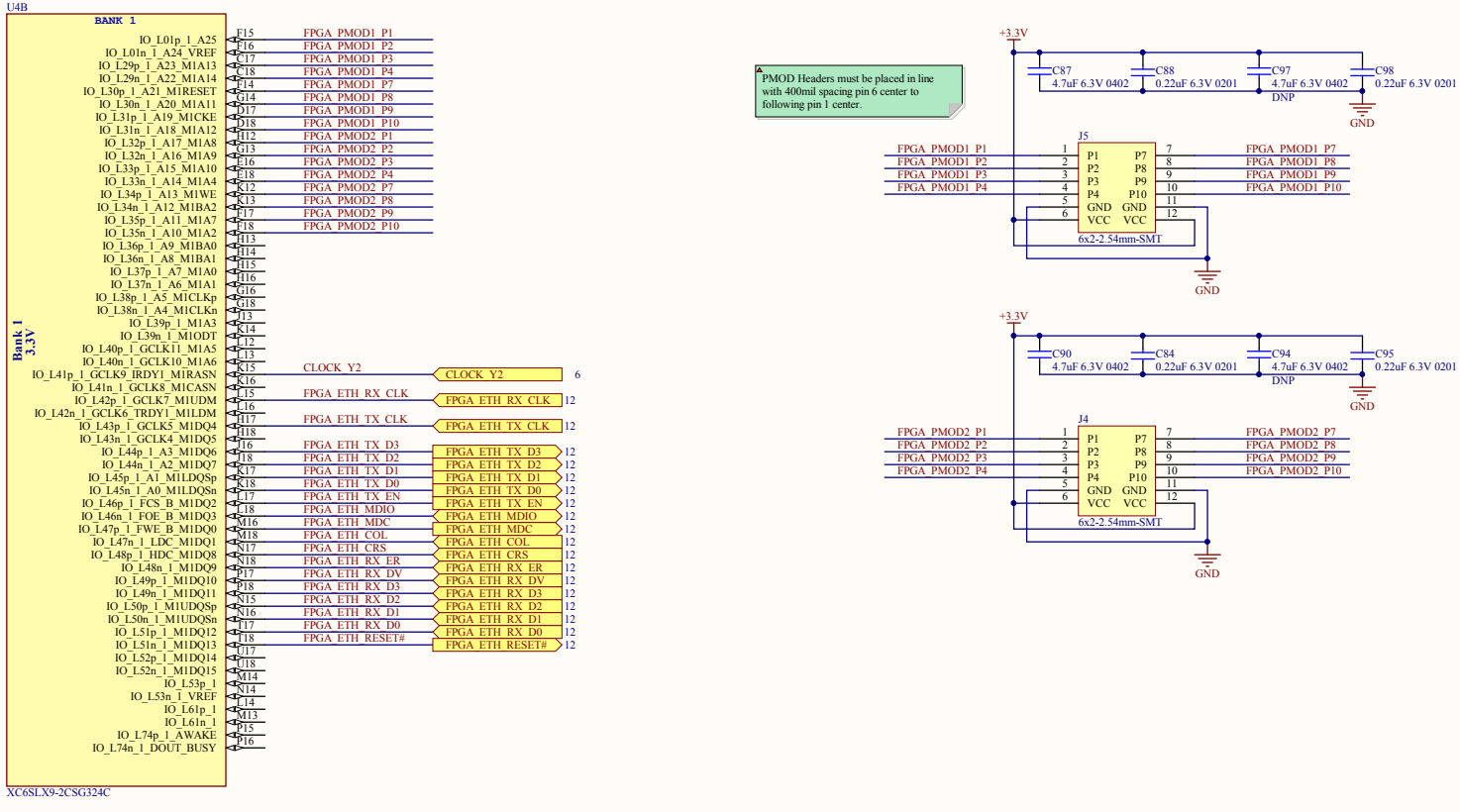
AVNET Avnet Engineering Services		
Title: Sheet 3 - Architecture		
Size: C	Document Number: S6-LX9-SCH-B	Rev: B
Date: 1/28/2011	Sheet 3 of 10	


U4A
BANK 0
Bank 0
3.3V
XC6SLX9-2CSG324
IO_L01p_0_HSWAPEN
IO_L01n_0_VREF
IO_L02p_0
IO_L02n_0
IO_L03p_0
IO_L03n_0
IO_L04p_0
IO_L04n_0
IO_L05p_0
IO_L05n_0
IO_L06p_0
IO_L06n_0
NC
NC
IO_L08p_0
IO_L08n_0_VREF
NC
NC
IO_L10p_0
IO_L10n_0
IO_L11p_0
IO_L11n_0
NC
NC
IO_L33p_0
IO_L33n_0
IO_L34p_0_GCLK19
IO_L34n_0_GCLK18
IO_L35p_0_GCLK17
IO_L35n_0_GCLK16
IO_L36p_0_GCLK15
IO_L36n_0_GCLK14
IO_L37p_0_GCLK13
IO_L37n_0_GCLK12
IO_L38p_0
IO_L38n_0_VREF
IO_L39p_0
IO_L39n_0
NC
NC
IO_L41p_0
IO_L41n_0
NC
NC
NC
NC
NC
NC
NC
NC
IO_L62p_0
IO_L62n_0_VREF
IO_L63p_0_SCP7
IO_L63n_0_SCP6
IO_L64p_0_SCP5
IO_L64n_0_SCP4
IO_L65p_0_SCP3
IO_L65n_0_SCP2
IO_L66p_0_SCP1
IO_L66n_0_SCP0
FPGA_HSWAPEN
R36
4K87 0402
+3.3V
SW1
4CH SMT DIP SW
RP1
4K7 DNP
GND
Use Internal Pull Down Resistor If Resistor Pack Is Not Installed.
CLOCK_Y3
6
G1
TEST PAD
G2
TEST PAD
X's are a "No ERC" directive to the Design Rule Checker to ignore rule violations.
Avnet Engineering Services
Title: Sheet 4 - FPGA Bank 0
Size: B
Document Number: S6-LX9-SCH-B
Rev: B
Date: 1/28/2011
Sheet 4 of 10


U4B
BANK 1
Bank 1
3.3V
IO_L01p_1_A25
IO_L01n_1_A24_VREF
IO_L29p_1_A23_M1A13
IO_L29n_1_A22_M1A14
IO_L30p_1_A21_M1RESET
IO_L30n_1_A20_M1A11
IO_L31p_1_A19_M1CKE
IO_L31n_1_A18_M1A12
IO_L32p_1_A17_M1A8
IO_L32n_1_A16_M1A9
IO_L33p_1_A15_M1A10
IO_L33n_1_A14_M1A4
IO_L34p_1_A13_M1WE
IO_L34n_1_A12_M1BA2
IO_L35p_1_A11_M1A7
IO_L35n_1_A10_M1A2
IO_L36p_1_A9_M1BA0
IO_L36n_1_A8_M1BA1
IO_L37p_1_A7_M1A0
IO_L37n_1_A6_M1A1
IO_L38p_1_A5_M1CLKp
IO_L38n_1_A4_M1CLKn
IO_L39p_1_M1A3
IO_L39n_1_M1ODT
IO_L40p_1_GCLK11_M1A5
IO_L40n_1_GCLK10_M1A6
IO_L41p_1_GCLK9_IRDY1_M1RASN
IO_L41n_1_GCLK8_M1CASN
IO_L42p_1_GCLK7_M1UDM
IO_L42n_1_GCLK6_TRDY1_M1LDM
IO_L43p_1_GCLK5_M1DQ4
IO_L43n_1_GCLK4_M1DQ5
IO_L44p_1_A3_M1DQ6
IO_L44n_1_A2_M1DQ7
IO_L45p_1_A1_M1LDQSp
IO_L45n_1_A0_M1LDQSn
IO_L46p_1_FCS_B_M1DQ2
IO_L46n_1_FOE_B_M1DQ3
IO_L47p_1_FWE_B_M1DQ0
IO_L47n_1_LDC_M1DQ1
IO_L48p_1_HDC_M1DQ8
IO_L48n_1_M1DQ9
IO_L49p_1_M1DQ10
IO_L49n_1_M1DQ11
IO_L50p_1_M1UDQSp
IO_L50n_1_M1UDQSn
IO_L51p_1_M1DQ12
IO_L51n_1_M1DQ13
IO_L52p_1_M1DQ14
IO_L52n_1_M1DQ15
IO_L53p_1
IO_L53n_1_VREF
IO_L61p_1
IO_L61n_1
IO_L74p_1_AWAKE
IO_L74n_1_DOUT_BUSY
F15 FPGA_PMOD1_P1
F16 FPGA_PMOD1_P2
C17 FPGA_PMOD1_P3
C18 FPGA_PMOD1_P4
F14 FPGA_PMOD1_P7
G14 FPGA_PMOD1_P8
D17 FPGA_PMOD1_P9
D18 FPGA_PMOD1_P10
H12 FPGA_PMOD2_P1
G13 FPGA_PMOD2_P2
E16 FPGA_PMOD2_P3
E18 FPGA_PMOD2_P4
K12 FPGA_PMOD2_P7
K13 FPGA_PMOD2_P8
F17 FPGA_PMOD2_P9
F18 FPGA_PMOD2_P10
H13
H14
H15
H16
G16
G18
J13
K14
J12
J13
K15 CLOCK_Y2
K16
L15 FPGA_ETH_RX_CLK
L16
H17 FPGA_ETH_TX_CLK
H18
J16 FPGA_ETH_TX_D3
J18 FPGA_ETH_TX_D2
K17 FPGA_ETH_TX_D1
K18 FPGA_ETH_TX_D0
L17 FPGA_ETH_TX_EN
L18 FPGA_ETH_MDIO
M16 FPGA_ETH_MDC
M18 FPGA_ETH_COL
N17 FPGA_ETH_CRS
N18 FPGA_ETH_RX_ER
P17 FPGA_ETH_RX_DV
P18 FPGA_ETH_RX_D3
N15 FPGA_ETH_RX_D2
N16 FPGA_ETH_RX_D1
T17 FPGA_ETH_RX_D0
T18 FPGA_ETH_RESET#
P17
P18
M14
N14
L14
M13
P15
P16
CLOCK_Y2 6
FPGA_ETH_RX_CLK 12
FPGA_ETH_TX_CLK 12
FPGA_ETH_TX_D3 12
FPGA_ETH_TX_D2 12
FPGA_ETH_TX_D1 12
FPGA_ETH_TX_D0 12
FPGA_ETH_TX_EN 12
FPGA_ETH_MDIO 12
FPGA_ETH_MDC 12
FPGA_ETH_COL 12
FPGA_ETH_CRS 12
FPGA_ETH_RX_ER 12
FPGA_ETH_RX_DV 12
FPGA_ETH_RX_D3 12
FPGA_ETH_RX_D2 12
FPGA_ETH_RX_D1 12
FPGA_ETH_RX_D0 12
FPGA_ETH_RESET# 12
XC6SLX9-2CSG324C
PMOD Headers must be placed in line with 400mil spacing pin 6 center to following pin 1 center.
+3.3V
C87 4.7uF 6.3V 0402
C88 0.22uF 6.3V 0201
C97 4.7uF 6.3V 0402 DNP
C98 0.22uF 6.3V 0201
GND
J5
FPGA_PMOD1_P1
FPGA_PMOD1_P2
FPGA_PMOD1_P3
FPGA_PMOD1_P4
P1 P7 P2 P8 P3 P9 P4 P10 GND GND VCC VCC
FPGA_PMOD1_P7
FPGA_PMOD1_P8
FPGA_PMOD1_P9
FPGA_PMOD1_P10
6x2-2.54mm-SMT
+3.3V
C90 4.7uF 6.3V 0402
C84 0.22uF 6.3V 0201
C94 4.7uF 6.3V 0402 DNP
C95 0.22uF 6.3V 0201
GND
J4
FPGA_PMOD2_P1
FPGA_PMOD2_P2
FPGA_PMOD2_P3
FPGA_PMOD2_P4
P1 P7 P2 P8 P3 P9 P4 P10 GND GND VCC VCC
FPGA_PMOD2_P7
FPGA_PMOD2_P8
FPGA_PMOD2_P9
FPGA_PMOD2_P10
6x2-2.54mm-SMT
GND
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AVNET
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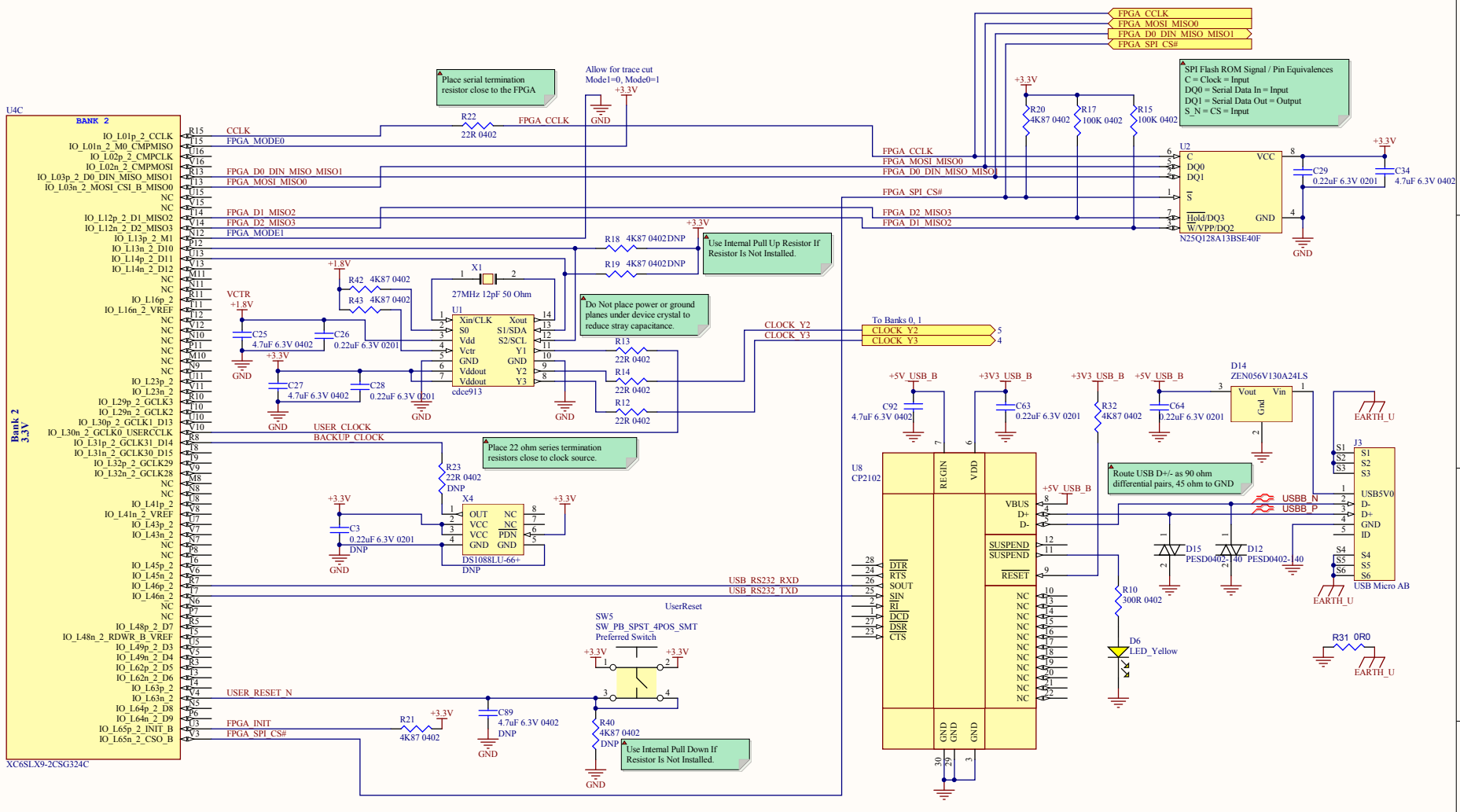
Title:
Sheet 5 - FPGA Bank 1
Size:
B
Document Number:
S6-LX9-SCH-B
Rev:
B
Date: 1/28/2011
Sheet 5 of 10


U4C
BANK 2
Bank 2
3.3V
XC6SLX9-2CSG324C
Place serial termination resistor close to the FPGA
Allow for trace cut
Mode1=0, Mode0=1
R22
22R 0402
FPGA_CCLK
GND
CCLK
FPGA_MODE0
FPGA_D0_DIN_MISO_MISO1
FPGA_MOSI_MISO0
FPGA_D1_MISO2
FPGA_D2_MISO3
FPGA_MODE1
R18 4K87 0402DNP
R19 4K87 0402DNP
Use Internal Pull Up Resistor If Resistor Is Not Installed.
+1.8V
R42 4K87 0402
R43 4K87 0402
VCTR
+1.8V
C25
4.7uF 6.3V 0402
C26
0.22uF 6.3V 0201
X1
27MHz 12pF 50 Ohm
U1
Xin/CLK
S0
Vdd
Vctr
GND
Vddout
Vddout
Xout
S1/SDA
S2/SCL
Y1
GND
Y2
Y3
cdce913
Do Not place power or ground planes under device crystal to reduce stray capacitance.
C27
4.7uF 6.3V 0402
C28
0.22uF 6.3V 0201
R13
22R 0402
R14
22R 0402
R12
22R 0402
CLOCK_Y2
CLOCK_Y3
To Banks 0, 1
USER_CLOCK
BACKUP_CLOCK
Place 22 ohm series termination resistors close to clock source.
R23
22R 0402
DNP
X4
OUT
VCC
VCC
GND
NC
NC
PDN
GND
DS1088LU-66+
DNP
C3
0.22uF 6.3V 0201
DNP
USB_RS232_RXD
USB_RS232_TXD
UserReset
SW5
SW_PB_SPST_4POS_SMT
Preferred Switch
USER_RESET_N
FPGA_INIT
FPGA_SPI_CS#
R21
4K87 0402
C89
4.7uF 6.3V 0402
DNP
R40
4K87 0402
DNP
Use Internal Pull Down If Resistor Is Not Installed.
FPGA_CCLK
FPGA_MOSI_MISO0
FPGA_D0_DIN_MISO_MISO1
FPGA_SPI_CS#
SPI Flash ROM Signal / Pin Equivalences
C = Clock = Input
DQ0 = Serial Data In = Input
DQ1 = Serial Data Out = Output
S_N = CS = Input
R20
4K87 0402
R17
100K 0402
R15
100K 0402
U2
C
DQ0
DQ1
S
Hold/DQ3
W/VPP/DQ2
VCC
GND
N25Q128A13BSE40F
C29
0.22uF 6.3V 0201
C34
4.7uF 6.3V 0402
FPGA_D2_MISO3
FPGA_D1_MISO2
U8
CP2102
REGIN
VDD
VBUS
D+
D-
SUSPEND
SUSPEND
RESET
DTR
RTS
SOUT
SIN
RI
DCD
DSR
CTS
GND
GND
GND
C92
4.7uF 6.3V 0402
C63
0.22uF 6.3V 0201
R32
4K87 0402
C64
0.22uF 6.3V 0201
D14
ZEN056V130A24LS
Vout
Vin
Gnd
Route USB D+/- as 90 ohm differential pairs, 45 ohm to GND
USBB_N
USBB_P
D15
PESD0402-140
D12
PESD0402-140
J3
USB5V0
D-
D+
GND
ID
USB Micro AB
R10
300R 0402
D6
LED_Yellow
R31 0R0
EARTH_U
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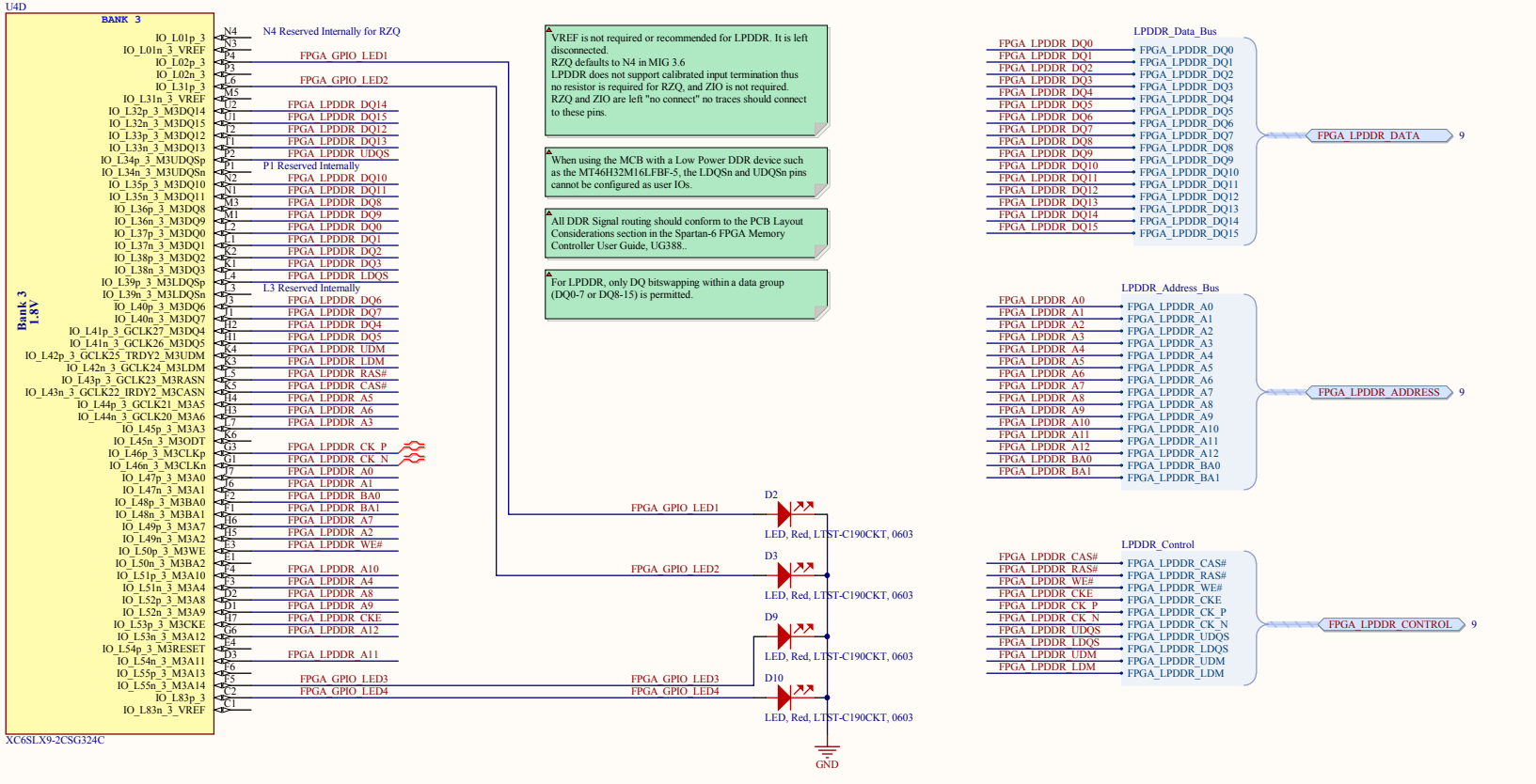
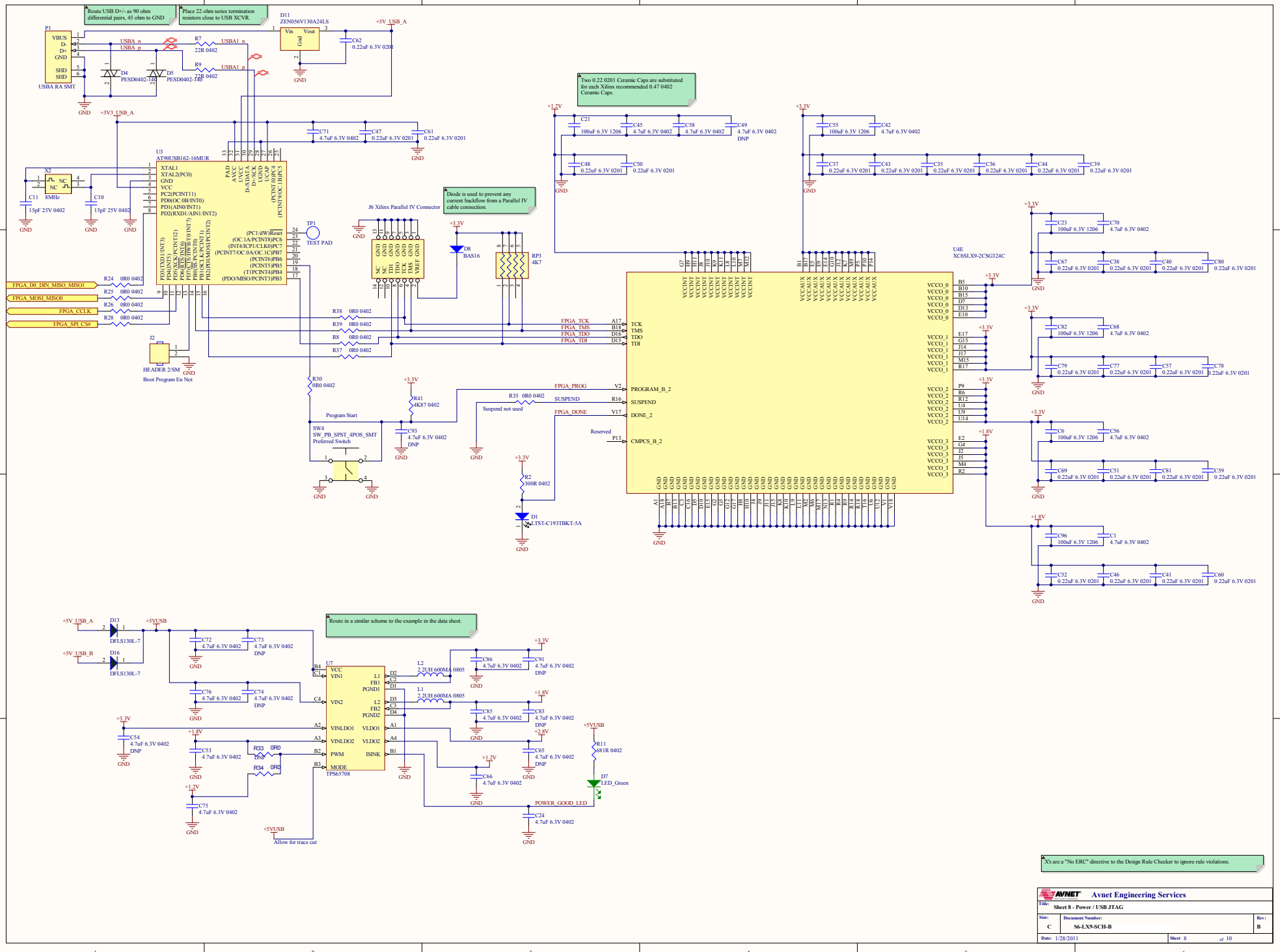
Avnet Engineering Services
Title: Sheet 6 - FPGA Bank 2
Size: B
Document Number: S6-LX9-SCH-B
Rev: B
Date: 1/28/2011
Sheet 6 of 10



Avnet Engineering Services	
Title:	Sheet 7 - FPGA Bank 3
Size: B	Document Number: S6-LX9-SCH-B
Rev:	B
Date: 1/28/2011	Sheet 7 of 10



Title:	Sheet 8 - Power / USB JTAG
Size: C	Document Number: S6-LX9-SCH-B
Rev:	B
Date: 1/28/2011	Sheet 8 of 10

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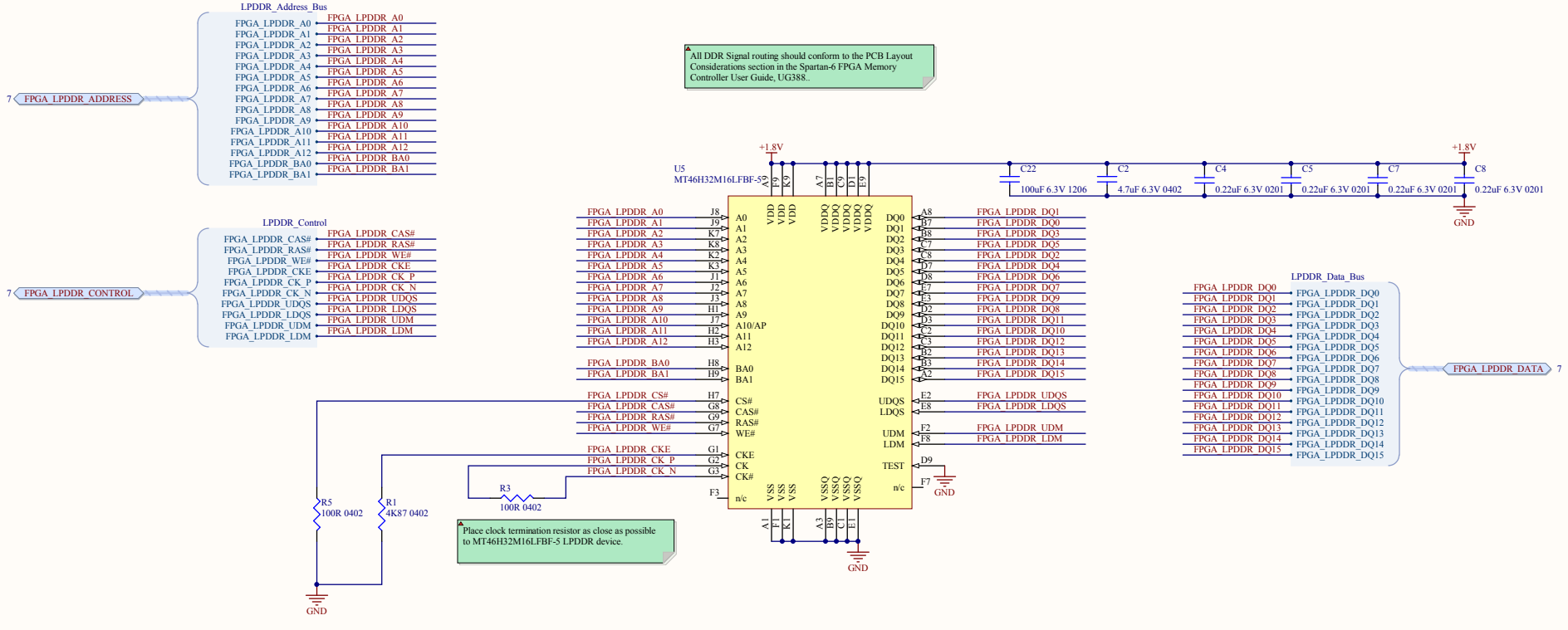
LPDDR_Address_Bus
7 FPGA_LPDDR_ADDRESS
FPGA_LPDDR_A0
FPGA_LPDDR_A1
FPGA_LPDDR_A2
FPGA_LPDDR_A3
FPGA_LPDDR_A4
FPGA_LPDDR_A5
FPGA_LPDDR_A6
FPGA_LPDDR_A7
FPGA_LPDDR_A8
FPGA_LPDDR_A9
FPGA_LPDDR_A10
FPGA_LPDDR_A11
FPGA_LPDDR_A12
FPGA_LPDDR_BA0
FPGA_LPDDR_BA1
LPDDR_Control
7 FPGA_LPDDR_CONTROL
FPGA_LPDDR_CAS#
FPGA_LPDDR_RAS#
FPGA_LPDDR_WE#
FPGA_LPDDR_CKE
FPGA_LPDDR_CK_P
FPGA_LPDDR_CK_N
FPGA_LPDDR_UDQS
FPGA_LPDDR_LDQS
FPGA_LPDDR_UDM
FPGA_LPDDR_LDM
All DDR Signal routing should conform to the PCB Layout Considerations section in the Spartan-6 FPGA Memory Controller User Guide, UG388..
U5
MT46H32M16LFBF-5
+1.8V
C22 100uF 6.3V 1206
C2 4.7uF 6.3V 0402
C4 0.22uF 6.3V 0201
C5 0.22uF 6.3V 0201
C7 0.22uF 6.3V 0201
C8 0.22uF 6.3V 0201
GND
R5 100R 0402
R1 4K87 0402
R3 100R 0402
Place clock termination resistor as close as possible to MT46H32M16LFBF-5 LPDDR device.
LPDDR_Data_Bus
FPGA_LPDDR_DATA 7
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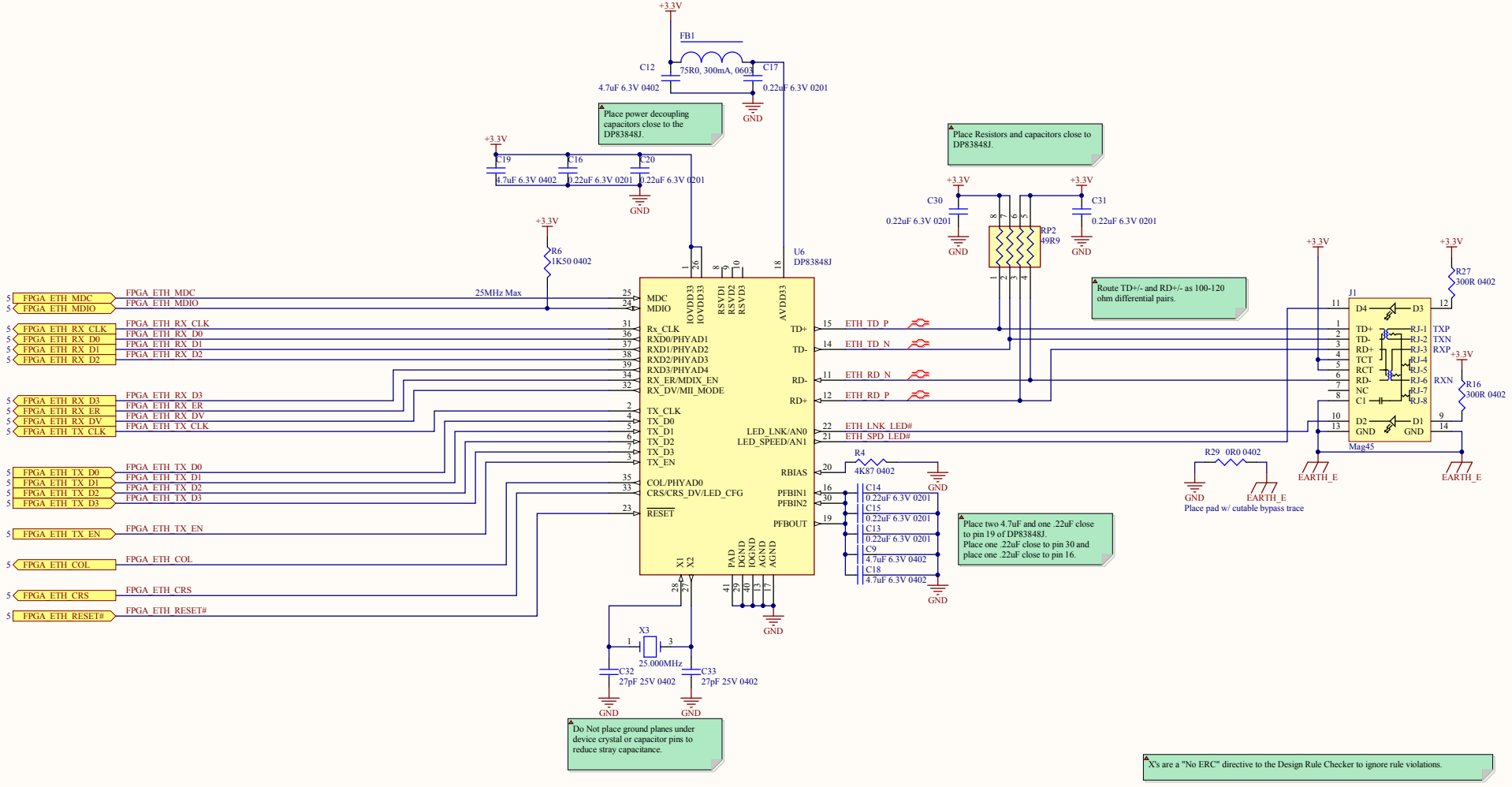
Avnet Engineering Services
Title: Sheet 9 - LPDDR Memory
Size: B
Document Number: S6-LX9-SCH-B
Rev: B
Date: 1/28/2011
Sheet 9 of 10



Avnet Engineering Services	
Title:	Sheet 10 - FPGA 10/100 Ethernet PHY
Size: B	Document Number: S6-LX9-SCH-B
Rev:	B
Date: 1/28/2011	Sheet 10 of 10