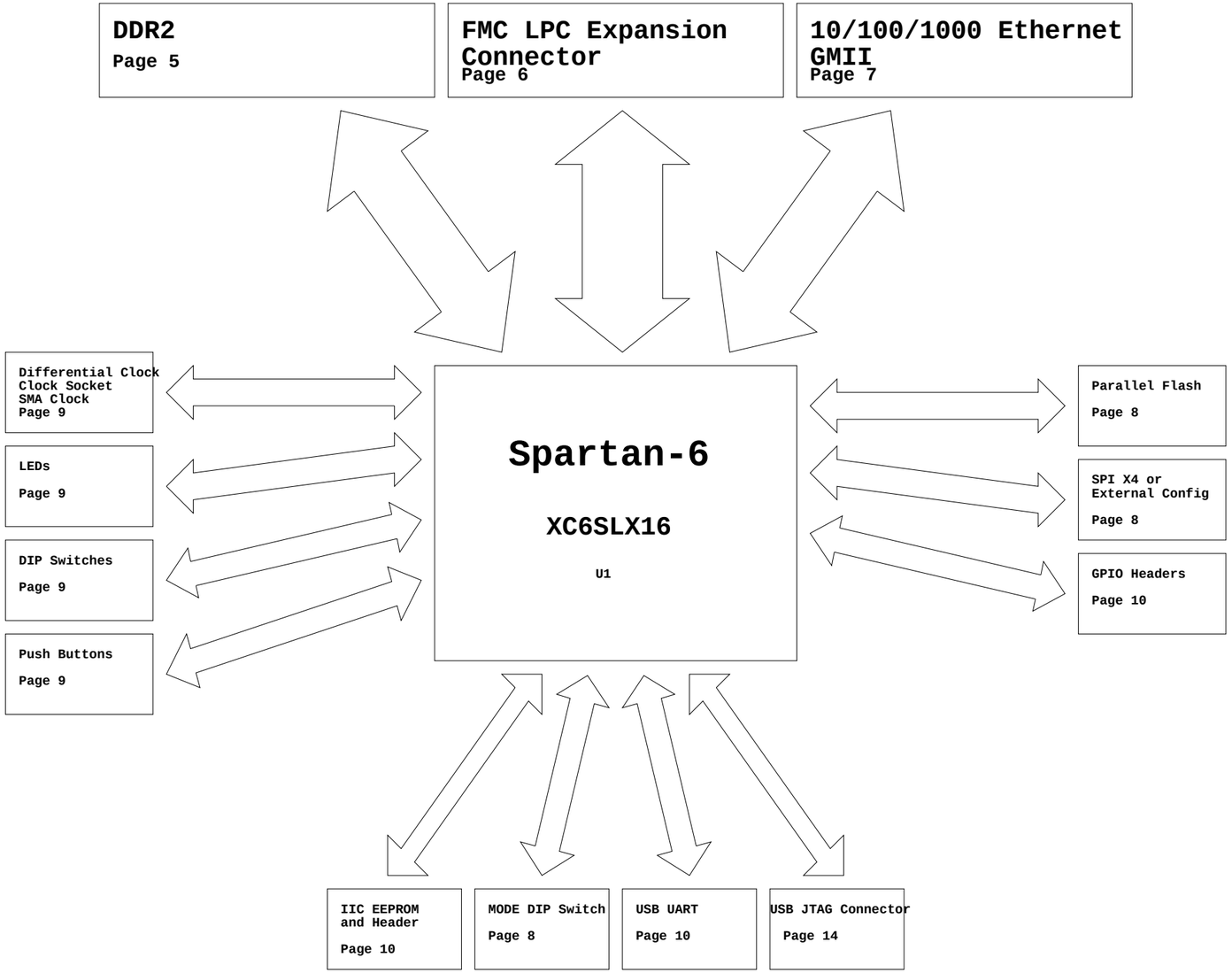
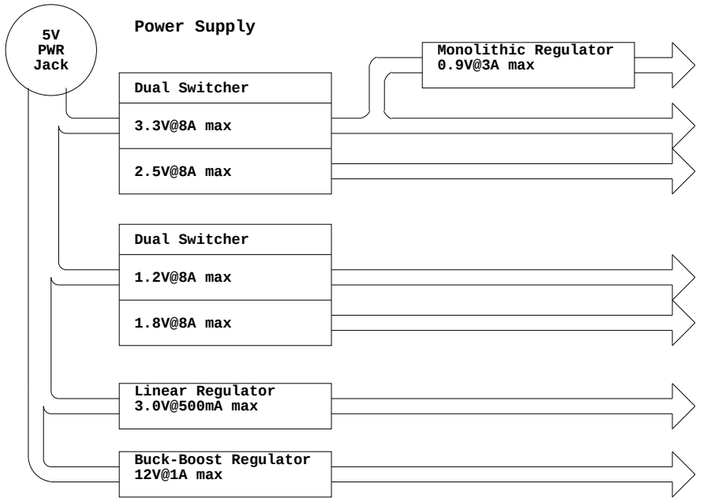
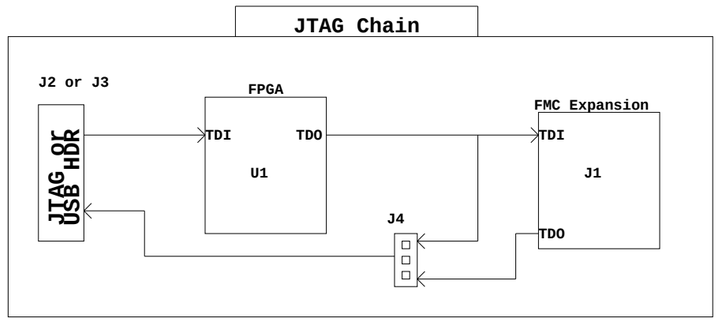
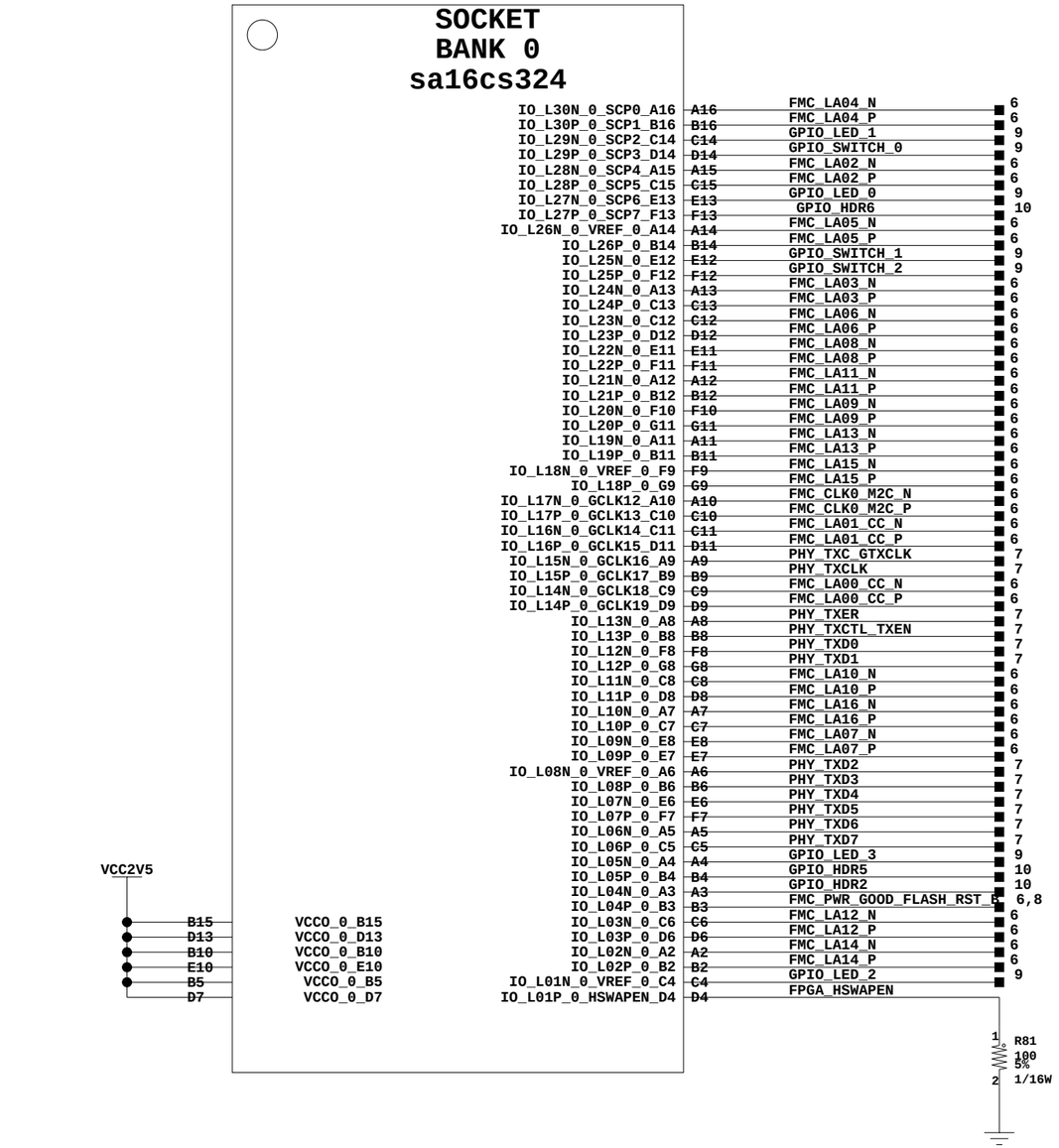


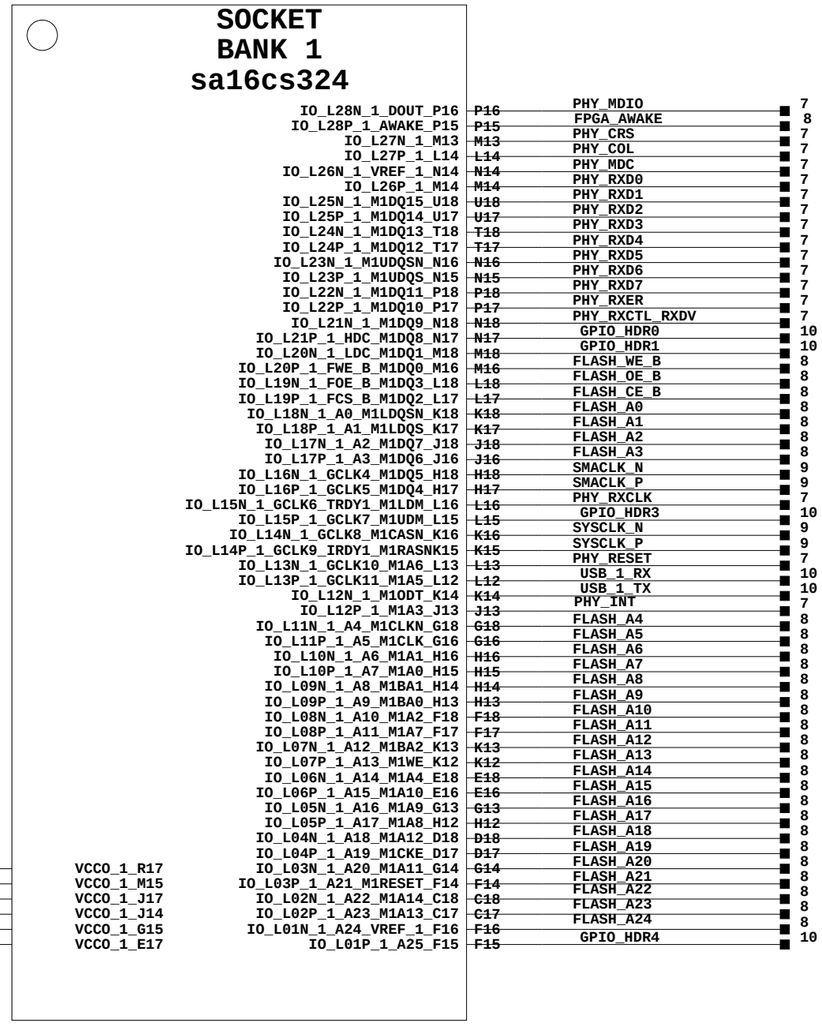


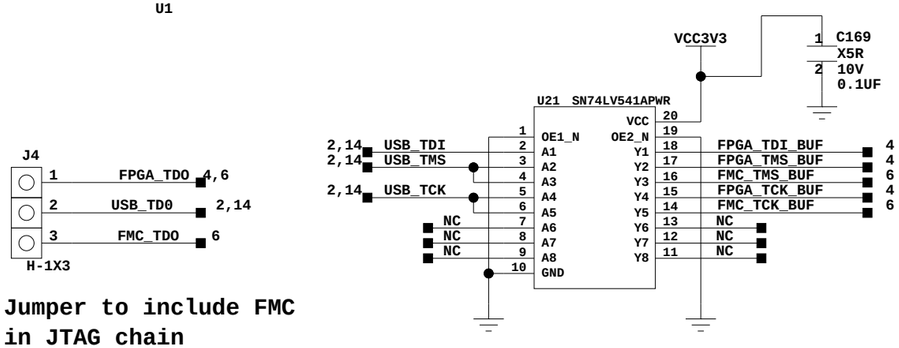


IIC Addresssing	
U5	0b1010000
J1	EEPROM: 0b1010010 Other Devices: 0bXXXXX10

Title:	SP601 Block Diagram SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431512 0381290 TSS0121 1280464
Date:	8-14-2009_16:47	Ver:	C
Sheet Size: B		Rev:	01
Sheet	1 of 16	Drawn By	BF





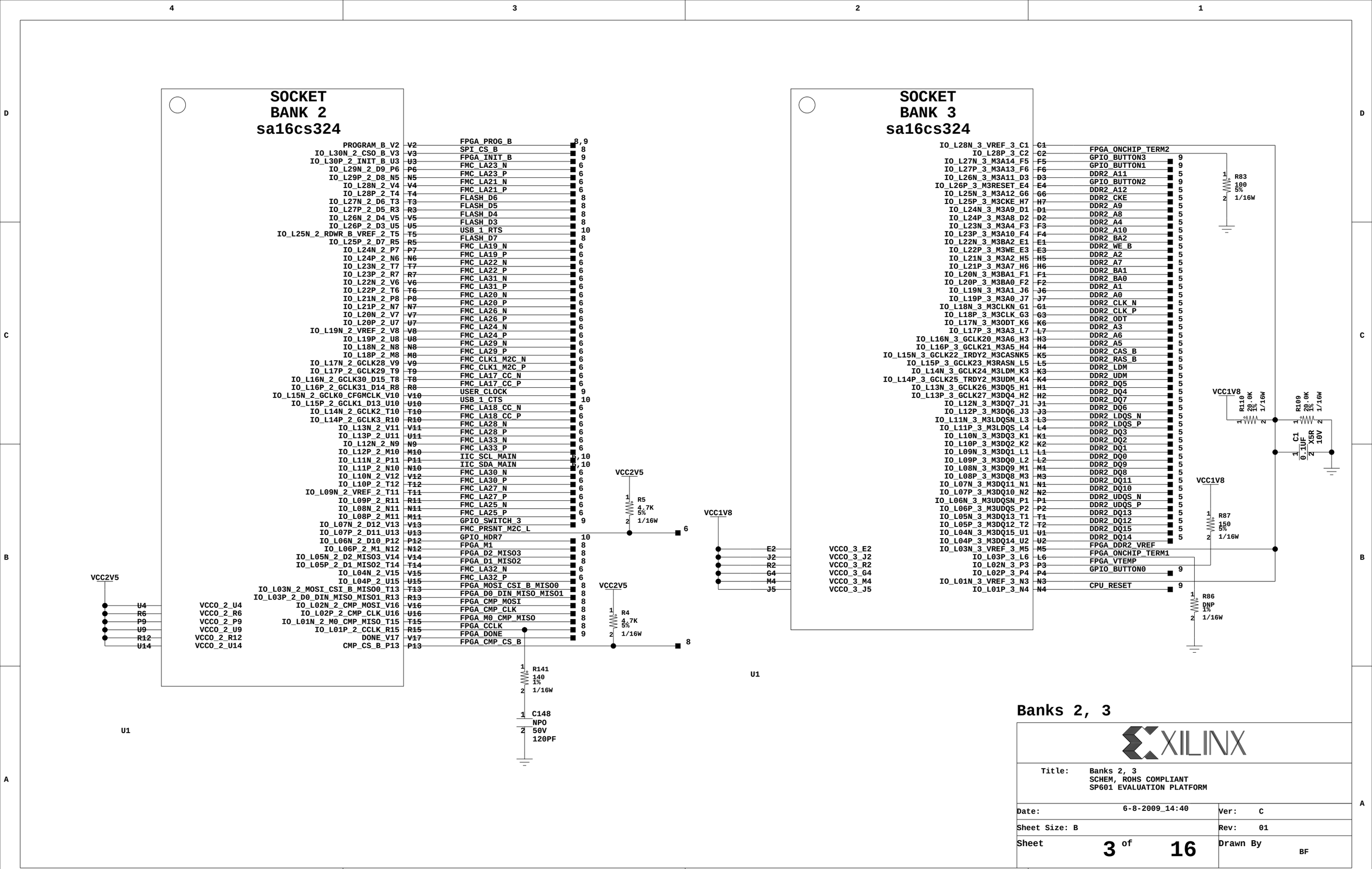


Jumper to include FMC in JTAG chain

Banks 0, 1

XILINX

Title:	Banks 0, 1 SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431512 0381290 TSS0121 1280464
Date:	6-8-2009_14:40	Ver:	C
Sheet Size: B		Rev:	01
Sheet	2 of 16	Drawn By	BF


SOCKET
BANK 2
sa16cs324
PROGRAM_B_V2 V2 FPGA_PROG_B 8,9
IO_L30N_2_CSO_B_V3 V3 SPI_CS_B 8
IO_L30P_2_INIT_B_U3 U3 FPGA_INIT_B 9
IO_L29N_2_D9_P6 P6 FMC_LA23_N 6
IO_L29P_2_D8_N5 N5 FMC_LA23_P 6
IO_L28N_2_V4 V4 FMC_LA21_N 6
IO_L28P_2_T4 T4 FMC_LA21_P 6
IO_L27N_2_D6_T3 T3 FLASH_D6 8
IO_L27P_2_D5_R3 R3 FLASH_D5 8
IO_L26N_2_D4_V5 V5 FLASH_D4 8
IO_L26P_2_D3_U5 U5 FLASH_D3 8
IO_L25N_2_RDWR_B_VREF_2_T5 T5 USB_1_RTS 10
IO_L25P_2_D7_R5 R5 FLASH_D7 8
IO_L24N_2_P7 P7 FMC_LA19_N 6
IO_L24P_2_N6 N6 FMC_LA19_P 6
IO_L23N_2_T7 T7 FMC_LA22_N 6
IO_L23P_2_R7 R7 FMC_LA22_P 6
IO_L22N_2_V6 V6 FMC_LA31_N 6
IO_L22P_2_T6 T6 FMC_LA31_P 6
IO_L21N_2_P8 P8 FMC_LA20_N 6
IO_L21P_2_N7 N7 FMC_LA20_P 6
IO_L20N_2_V7 V7 FMC_LA26_N 6
IO_L20P_2_U7 U7 FMC_LA26_P 6
IO_L19N_2_VREF_2_V8 V8 FMC_LA24_N 6
IO_L19P_2_U8 U8 FMC_LA24_P 6
IO_L18N_2_N8 N8 FMC_LA29_N 6
IO_L18P_2_M8 M8 FMC_LA29_P 6
IO_L17N_2_GCLK28_V9 V9 FMC_CLK1_M2C_N 6
IO_L17P_2_GCLK29_T9 T9 FMC_CLK1_M2C_P 6
IO_L16N_2_GCLK30_D15_T8 T8 FMC_LA17_CC_N 6
IO_L16P_2_GCLK31_D14_R8 R8 FMC_LA17_CC_P 6
IO_L15N_2_GCLK0_CFGMCLK_V10 V10 USER_CLOCK 9
IO_L15P_2_GCLK1_D13_U10 U10 USB_1_CTS 10
IO_L14N_2_GCLK2_T10 T10 FMC_LA18_CC_N 6
IO_L14P_2_GCLK3_R10 R10 FMC_LA18_CC_P 6
IO_L13N_2_V11 V11 FMC_LA28_N 6
IO_L13P_2_U11 U11 FMC_LA28_P 6
IO_L12N_2_N9 N9 FMC_LA33_N 6
IO_L12P_2_M10 M10 FMC_LA33_P 6
IO_L11N_2_P11 P11 IIC_SCL_MAIN 9,10
IO_L11P_2_N10 N10 IIC_SDA_MAIN 9,10
IO_L10N_2_V12 V12 FMC_LA30_N 6
IO_L10P_2_T12 T12 FMC_LA30_P 6
IO_L09N_2_VREF_2_T11 T11 FMC_LA27_N 6
IO_L09P_2_R11 R11 FMC_LA27_P 6
IO_L08N_2_N11 N11 FMC_LA25_N 6
IO_L08P_2_M11 M11 FMC_LA25_P 6
IO_L07N_2_D12_V13 V13 GPIO_SWITCH_3 9
IO_L07P_2_D11_U13 U13 FMC_PRSNT_M2C_L
IO_L06N_2_D10_P12 P12 GPIO_HDR7 10
IO_L06P_2_M1_N12 N12 FPGA_M1 8
IO_L05N_2_D2_MISO3_V14 V14 FPGA_D2_MISO3 8
IO_L05P_2_D1_MISO2_T14 T14 FPGA_D1_MISO2 8
IO_L04N_2_V15 V15 FMC_LA32_N 6
IO_L04P_2_U15 U15 FMC_LA32_P 6
IO_L03N_2_MOSI_CSI_B_MISO0_T13 T13 FPGA_MOSI_CSI_B_MISO0 8
IO_L03P_2_D0_DIN_MISO_MISO1_R13 R13 FPGA_D0_DIN_MISO_MISO1 8
IO_L02N_2_CMP_MOSI_V16 V16 FPGA_CMP_MOSI 8
IO_L02P_2_CMP_CLK_U16 U16 FPGA_CMP_CLK 8
IO_L01N_2_M0_CMP_MISO_T15 T15 FPGA_M0_CMP_MISO 8
IO_L01P_2_CCLK_R15 R15 FPGA_CCLK 8
DONE_V17 V17 FPGA_DONE 9
CMP_CS_B_P13 P13 FPGA_CMP_CS_B 8
VCC2V5
R5 4.7K 5% 1/16W
6
VCC2V5
R4 4.7K 5% 1/16W
8
R141 140 1% 1/16W
C148 NPO 50V 120PF
VCC2V5
U4 R6 P9 U9 R12 U14
VCCO_2_U4 VCCO_2_R6 VCCO_2_P9 VCCO_2_U9 VCCO_2_R12 VCCO_2_U14
U1
SOCKET
BANK 3
sa16cs324
IO_L28N_3_VREF_3_C1 C1
IO_L28P_3_C2 C2
IO_L27N_3_M3A14_F5 F5 GPIO_BUTTON3 9
IO_L27P_3_M3A13_F6 F6 GPIO_BUTTON1 9
IO_L26N_3_M3A11_D3 D3 DDR2_A11 5
IO_L26P_3_M3RESET_E4 E4 GPIO_BUTTON2 9
IO_L25N_3_M3A12_G6 G6 DDR2_A12 5
IO_L25P_3_M3CKE_H7 H7 DDR2_CKE 5
IO_L24N_3_M3A9_D1 D1 DDR2_A9 5
IO_L24P_3_M3A8_D2 D2 DDR2_A8 5
IO_L23N_3_M3A4_F3 F3 DDR2_A4 5
IO_L23P_3_M3A10_F4 F4 DDR2_A10 5
IO_L22N_3_M3BA2_E1 E1 DDR2_BA2 5
IO_L22P_3_M3WE_E3 E3 DDR2_WE_B 5
IO_L21N_3_M3A2_H5 H5 DDR2_A2 5
IO_L21P_3_M3A7_H6 H6 DDR2_A7 5
IO_L20N_3_M3BA1_F1 F1 DDR2_BA1 5
IO_L20P_3_M3BA0_F2 F2 DDR2_BA0 5
IO_L19N_3_M3A1_J6 J6 DDR2_A1 5
IO_L19P_3_M3A0_J7 J7 DDR2_A0 5
IO_L18N_3_M3CLKN_G1 G1 DDR2_CLK_N 5
IO_L18P_3_M3CLK_G3 G3 DDR2_CLK_P 5
IO_L17N_3_M3ODT_K6 K6 DDR2_ODT 5
IO_L17P_3_M3A3_L7 L7 DDR2_A3 5
IO_L16N_3_GCLK20_M3A6_H3 H3 DDR2_A6 5
IO_L16P_3_GCLK21_M3A5_H4 H4 DDR2_A5 5
IO_L15N_3_GCLK22_IRDY2_M3CASNK5 K5 DDR2_CAS_B 5
IO_L15P_3_GCLK23_M3RASN_L5 L5 DDR2_RAS_B 5
IO_L14N_3_GCLK24_M3LDM_K3 K3 DDR2_LDM 5
IO_L14P_3_GCLK25_TRDY2_M3UDM_K4 K4 DDR2_UDM 5
IO_L13N_3_GCLK26_M3DQ5_H1 H1 DDR2_DQ5 5
IO_L13P_3_GCLK27_M3DQ4_H2 H2 DDR2_DQ4 5
IO_L12N_3_M3DQ7_J1 J1 DDR2_DQ7 5
IO_L12P_3_M3DQ6_J3 J3 DDR2_DQ6 5
IO_L11N_3_M3LDQSN_L3 L3 DDR2_LDQS_N 5
IO_L11P_3_M3LDQS_L4 L4 DDR2_LDQS_P 5
IO_L10N_3_M3DQ3_K1 K1 DDR2_DQ3 5
IO_L10P_3_M3DQ2_K2 K2 DDR2_DQ2 5
IO_L09N_3_M3DQ1_L1 L1 DDR2_DQ1 5
IO_L09P_3_M3DQ0_L2 L2 DDR2_DQ0 5
IO_L08N_3_M3DQ9_M1 M1 DDR2_DQ9 5
IO_L08P_3_M3DQ8_M3 M3 DDR2_DQ8 5
IO_L07N_3_M3DQ11_N1 N1 DDR2_DQ11 5
IO_L07P_3_M3DQ10_N2 N2 DDR2_DQ10 5
IO_L06N_3_M3UDQSN_P1 P1 DDR2_UDQS_N 5
IO_L06P_3_M3UDQS_P2 P2 DDR2_UDQS_P 5
IO_L05N_3_M3DQ13_T1 T1 DDR2_DQ13 5
IO_L05P_3_M3DQ12_T2 T2 DDR2_DQ12 5
IO_L04N_3_M3DQ15_U1 U1 DDR2_DQ15 5
IO_L04P_3_M3DQ14_U2 U2 DDR2_DQ14 5
IO_L03N_3_VREF_3_M5 M5 FPGA_DDR2_VREF
IO_L03P_3_L6 L6 FPGA_ONCHIP_TERM1
IO_L02N_3_P3 P3 FPGA_VTEMP
IO_L02P_3_P4 P4 GPIO_BUTTON0 9
IO_L01N_3_VREF_3_N3 N3
IO_L01P_3_N4 N4 CPU_RESET 9
FPGA_ONCHIP_TERM2
R83 100 5% 1/16W
VCC1V8
R87 150 5% 1/16W
R86 DNP 1% 1/16W
VCC1V8
R110 20.0K 1% 1/16W
R109 20.0K 1% 1/16W
C1 0.1UF X5R 10V
VCC1V8
E2 J2 R2 G4 M4 J5
VCCO_3_E2 VCCO_3_J2 VCCO_3_R2 VCCO_3_G4 VCCO_3_M4 VCCO_3_J5
U1
Banks 2, 3
XILINX
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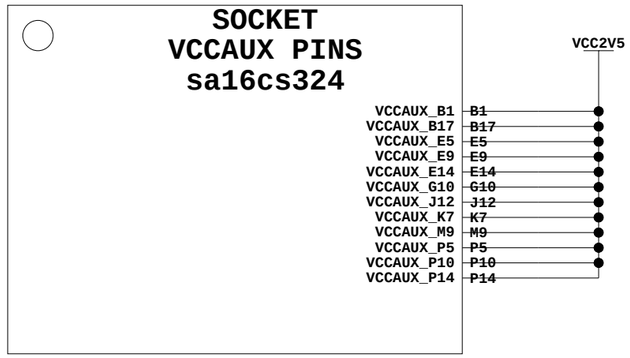
SCHEM, ROHS COMPLIANT
SP601 EVALUATION PLATFORM
Date: 6-8-2009_14:40
Ver: C
Sheet Size: B
Rev: 01
Sheet 3 of 16
Drawn By BF



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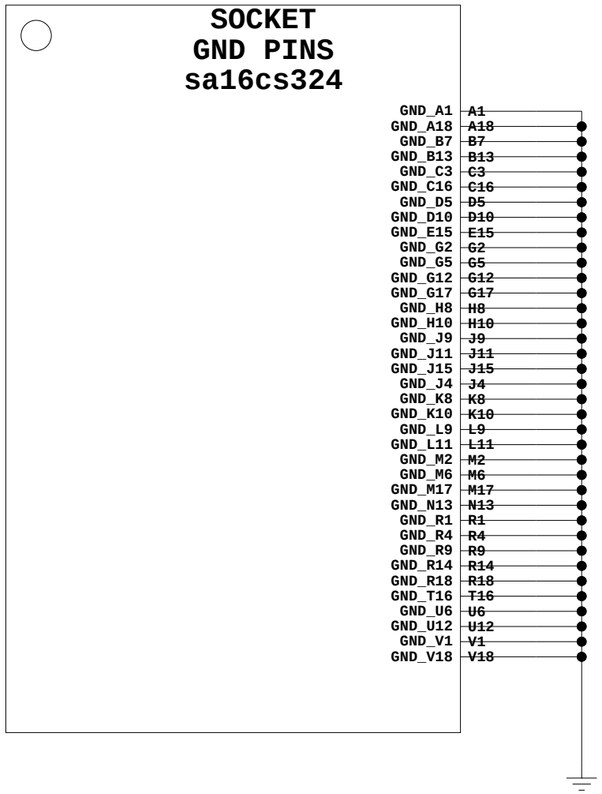

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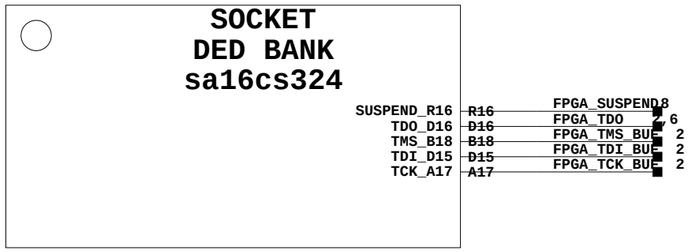

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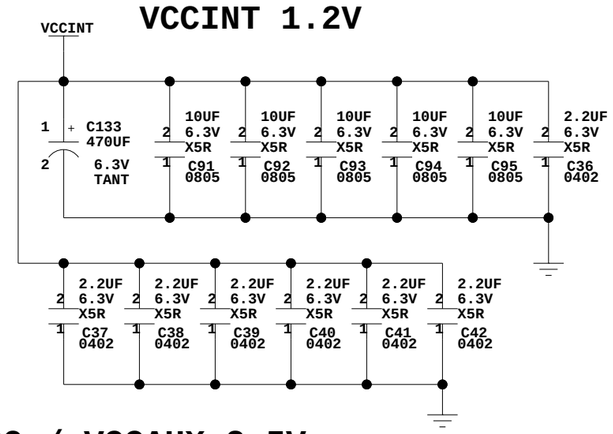

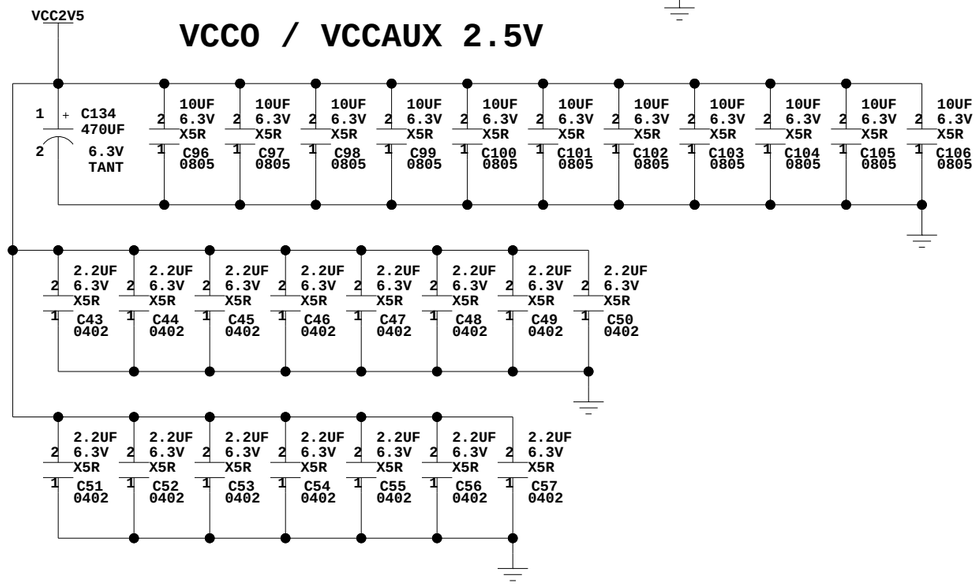

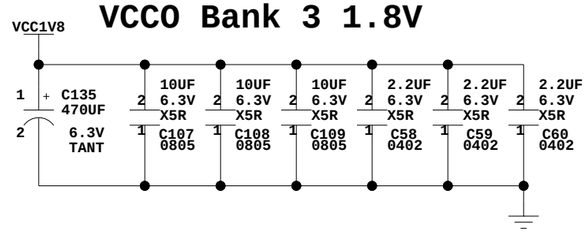

GND Bank, Decoupling caps

XILINX

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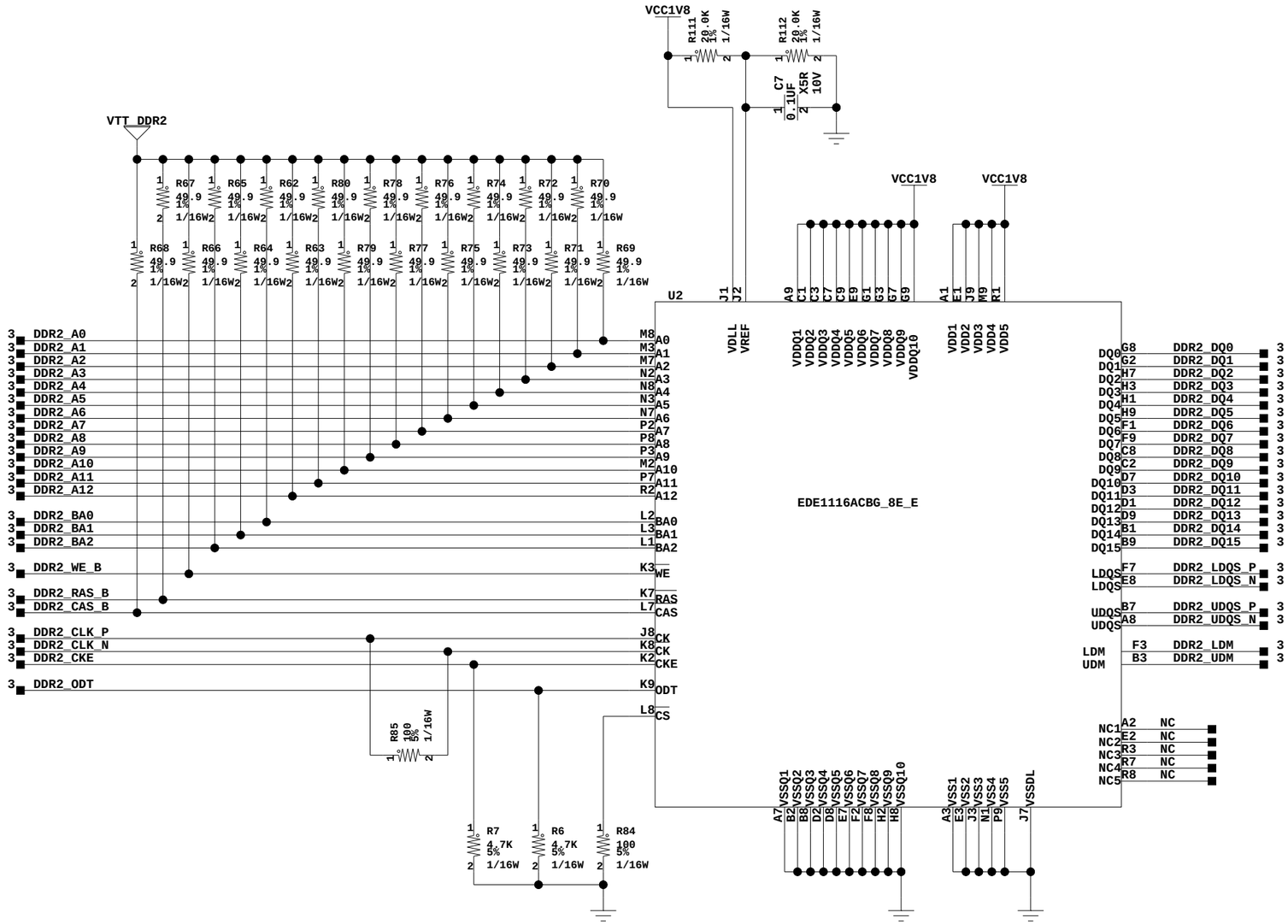
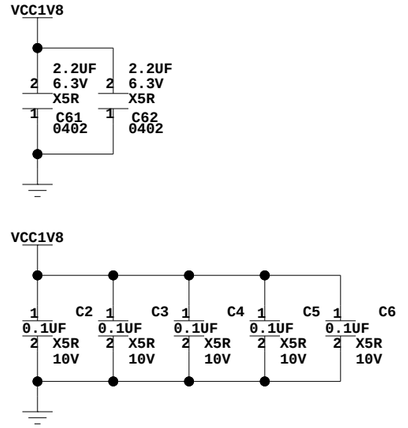
Sheet Size: B		Rev:	01
Sheet	4 of 16	Drawn By	BF



DDR2 Decoupling



DDR2 SDRAM

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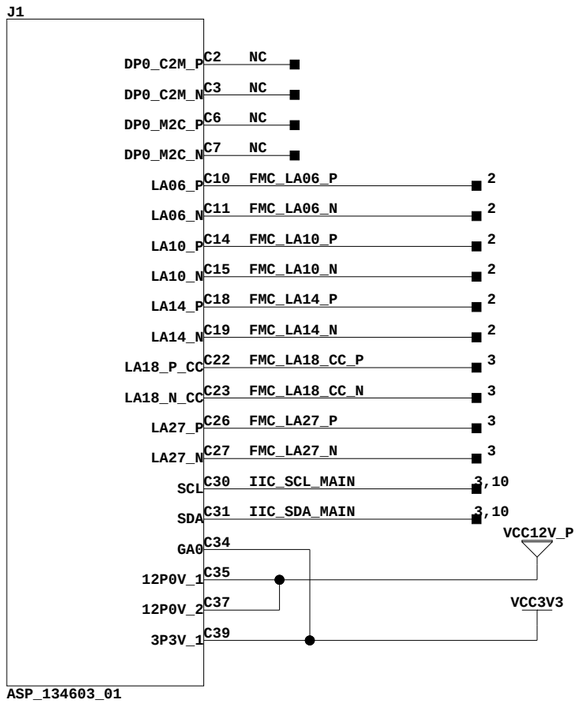
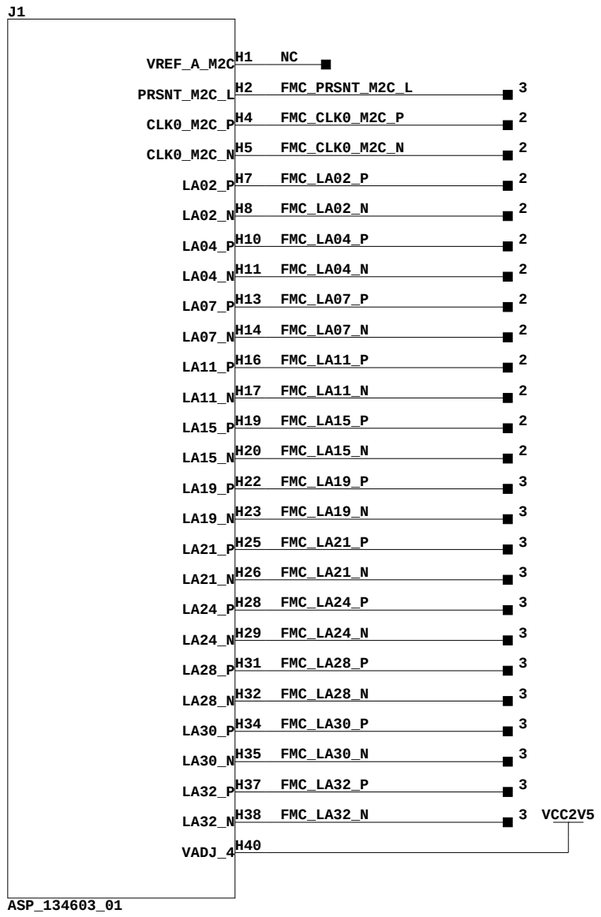
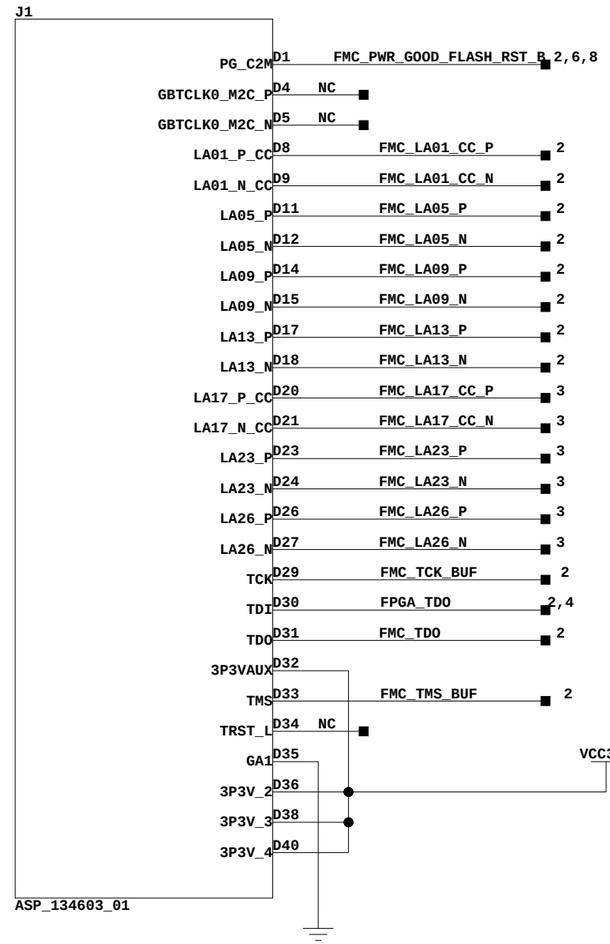
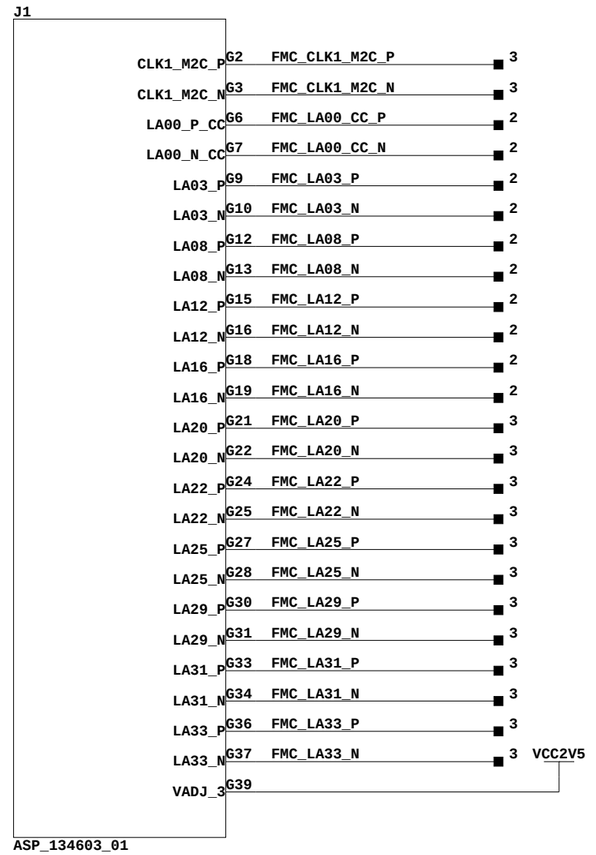
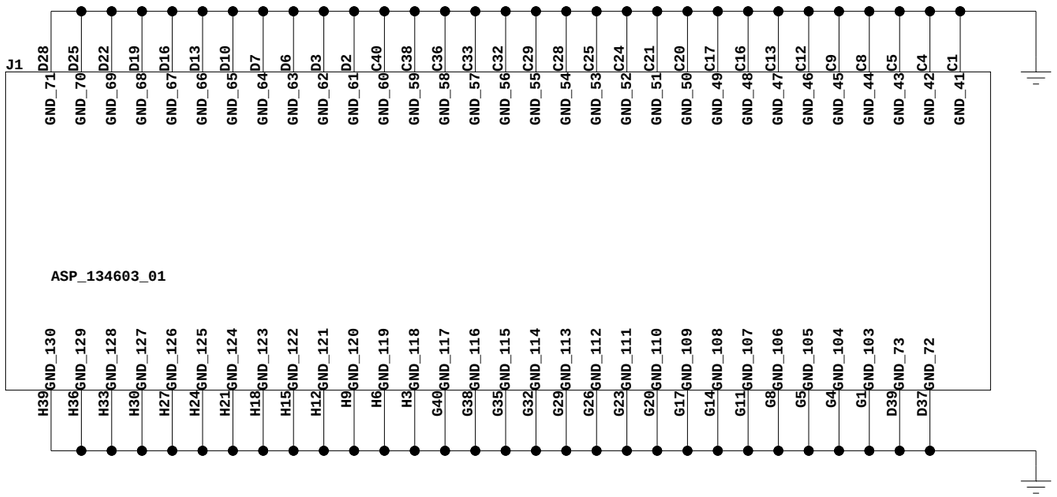
Sheet Size: B		Rev:	01
Sheet	5 of 16	Drawn By	BF

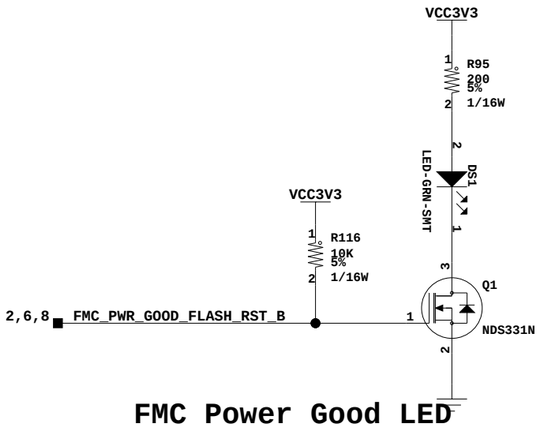




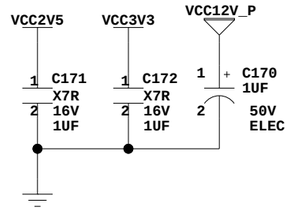








FMC Power Good LED



ANSI/VITA 57.1-2008 Version 1.1 FMC LPC Connector

XILINX

Title:	FMC LPC Connector SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM		
Date:	6-8-2009_14:40	Ver:	C
Sheet Size: B		Rev:	01
Sheet	6 of 16	Drawn By	BF

The PHY MDIP Pins below are
Media Dependent Interface Pins (MDIP),
and are all bidirectional pins.

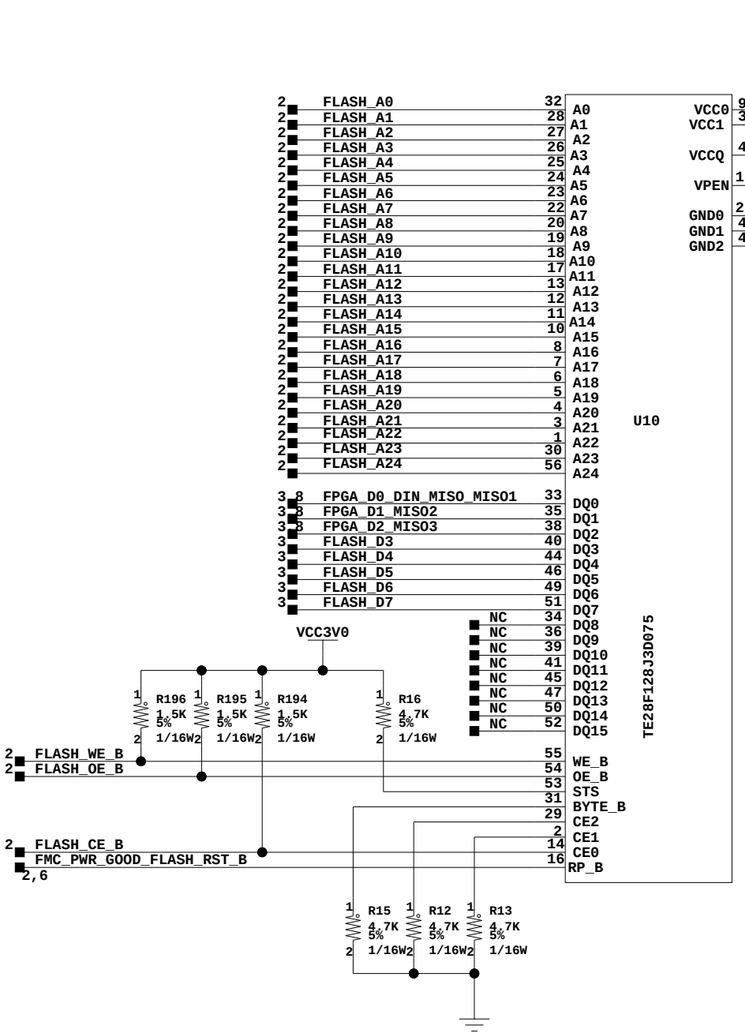
Pin to Constant Mapping	
Pin	Bit [2:0]
VCC2V5	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
GND	000

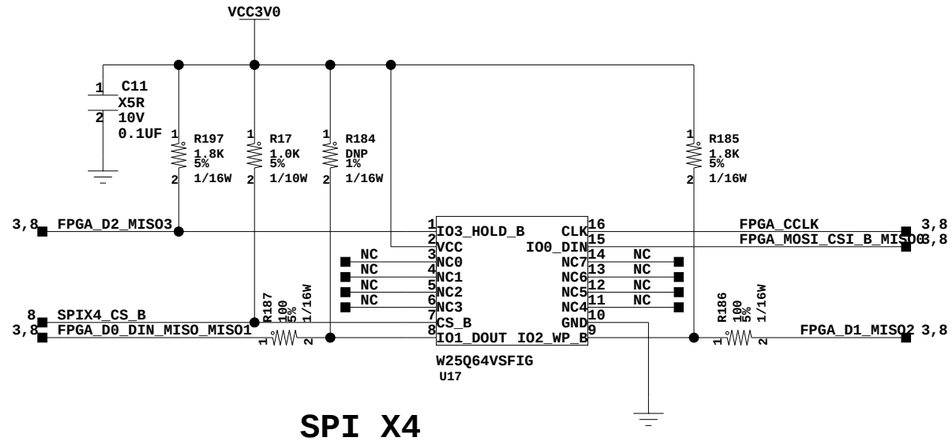
Pin	Bit[2]	Bit[1]	Bit[0]		
CFG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	111	PHYAddr "00111". Don't advertise the PAUSE bit
CFG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000	
CFG2	ANEG[3]	ANEG[2]	ANEG[1]	111	Auto-Neg en, advertise all caps; prefer slave. Auto crossover enabled. 125 CLK option disabled.
CFG3	ANEG[0]	ENA_XC	DIS_125	111	
CFG4	HWCFG_MD[2]	HWCFG_MD[1]	HWCFG_MD[0]	111	GMII to Cu mode. Fiber/copper auto-detect diasabled. Sleep mode disabled.
CFG5	DIS_FC	DIS_SLEEP	HWCFG_MD[3]	111	
CFG6	SEL_BDT	INT_POL	75/50 OHM	010	MDC/MDIO selected. Active LOW interrupt 50Ohm SERDES option.

10/100/1000 PHY

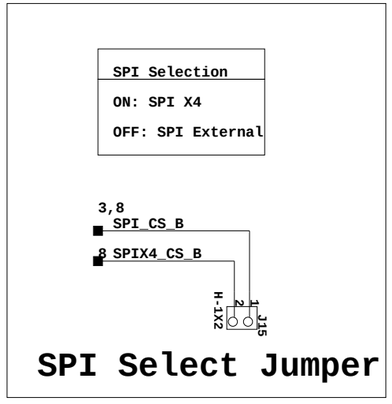
XILINX

Title:	10/100/1000 PHY SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM		
Date:	6-8-2009_14:40	Ver:	C
Sheet Size: B		Rev:	01
Sheet	7 of 16	Drawn By	BF

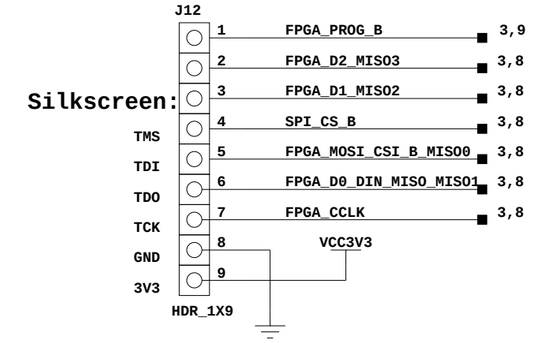




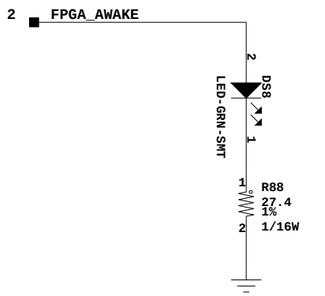
SPI X4



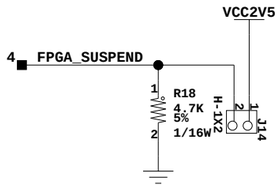
SPI Select Jumper

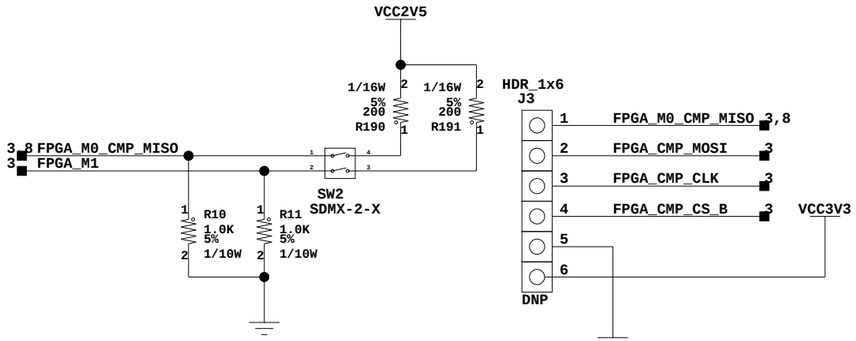


SPI Program Header



Suspend Jumper





Mode pin DIP switches

Parallel Flash, SPI, CMP, Mode, and Suspend

XILINX

Title:	Parallel Flash, SPI, CMP, Mode, and Suspend SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM
Date: 6-8-2009_14:40	Ver: C
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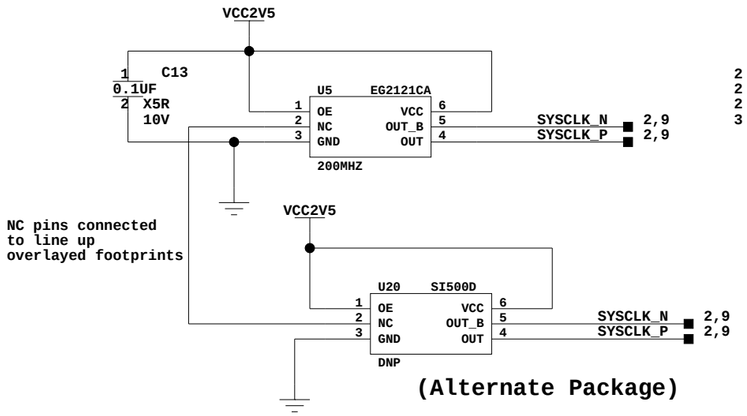
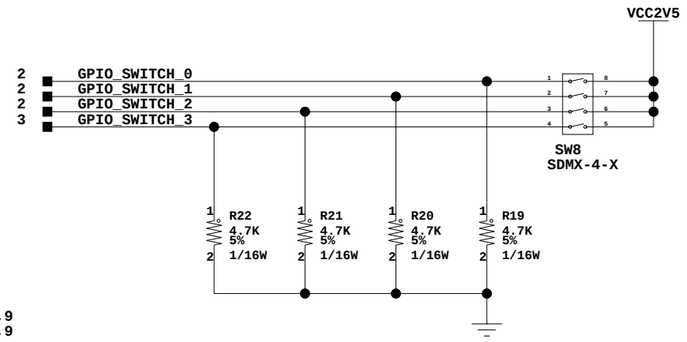
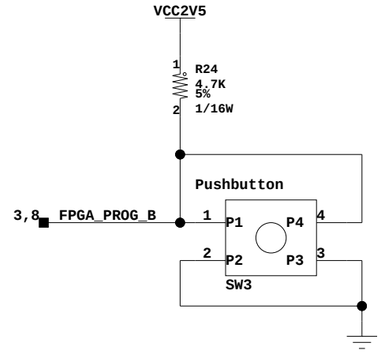
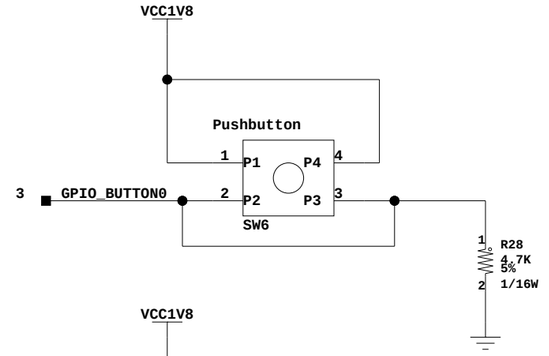
Sheet 8 of 16	Drawn By BF

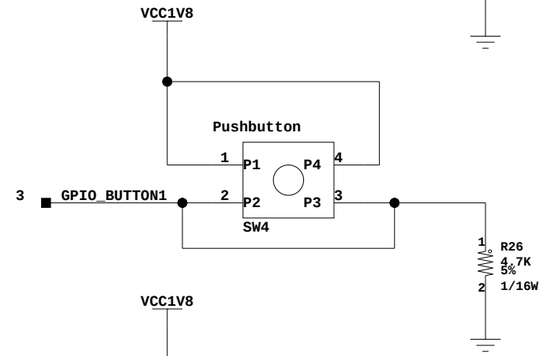


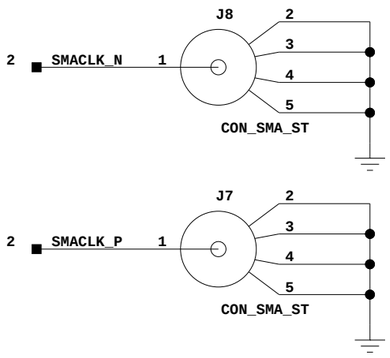
Differential System Clock



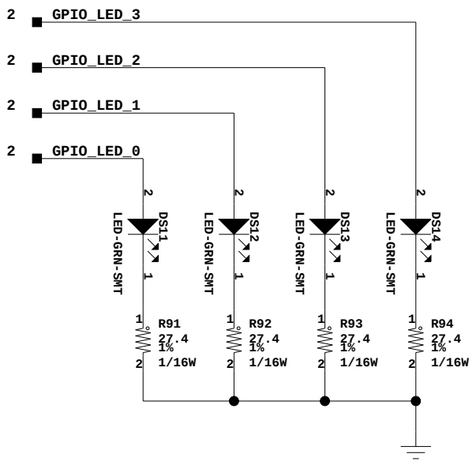


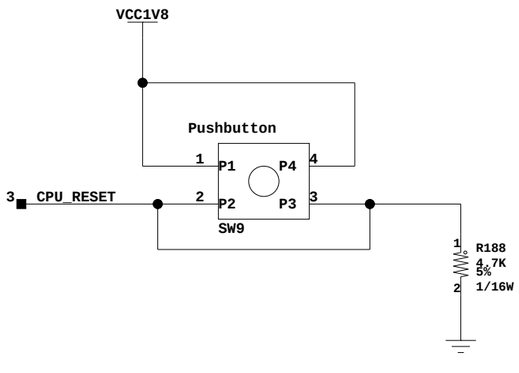


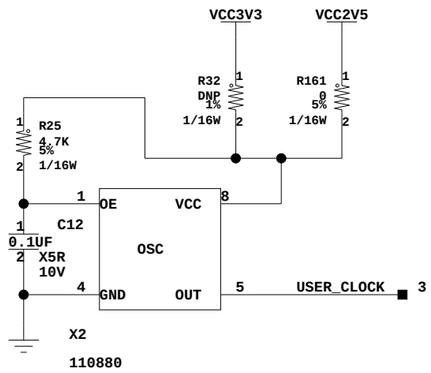




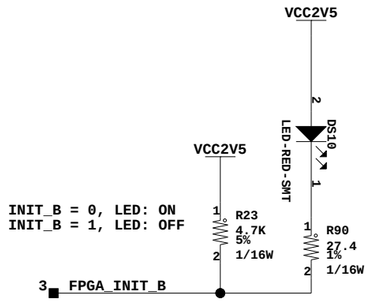
SMA Differential Clock

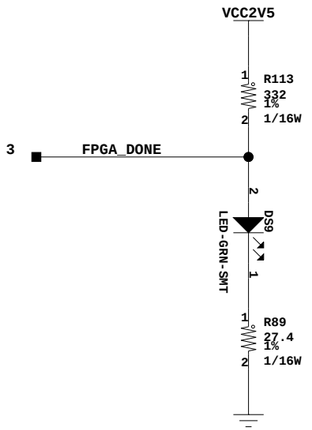






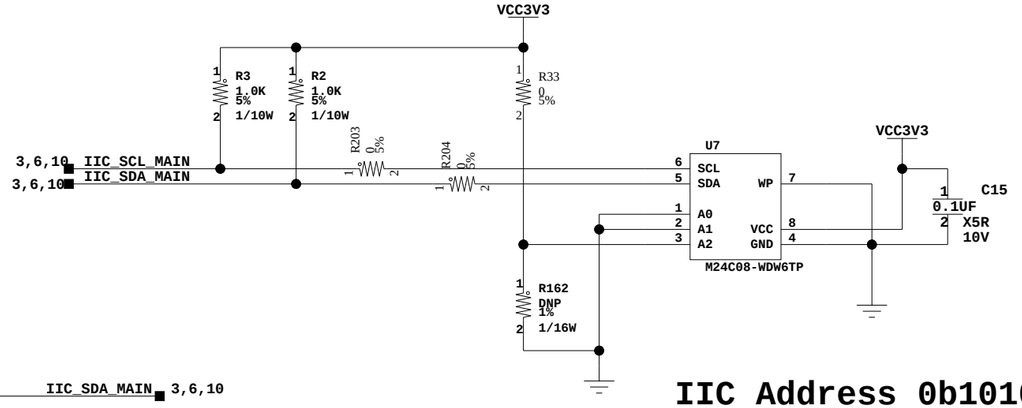
Single Ended User Clock

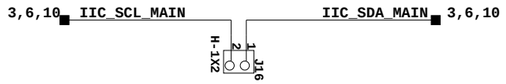




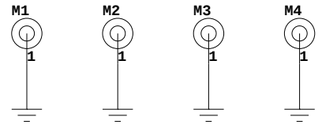
Clocks, LEDs, Buttons, Switches

Title:	Clocks, LEDs, Buttons, Switches SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM		
Date:	6-8-2009_14:40	Ver:	C
Sheet Size: B		Rev:	01
Sheet	9 of 16	Drawn By	BF

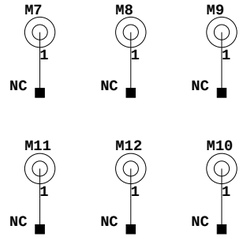




IIC Address 0b1010000



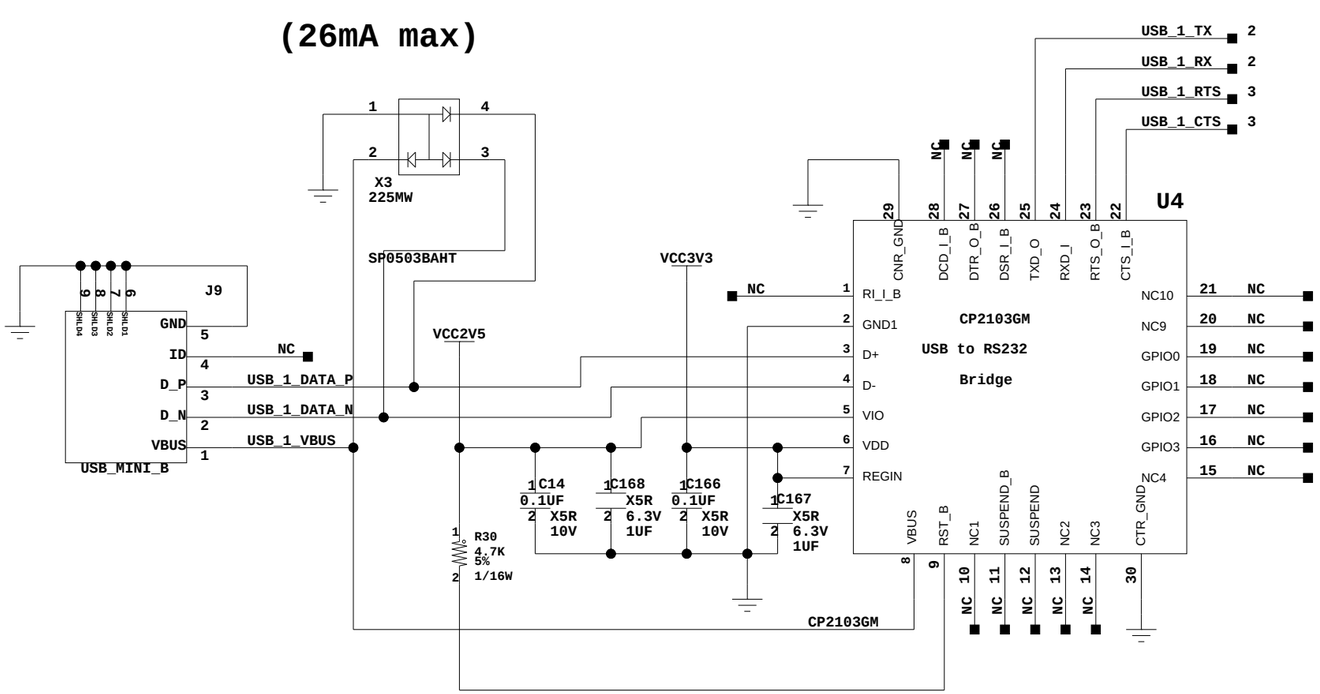
Mounting Holes

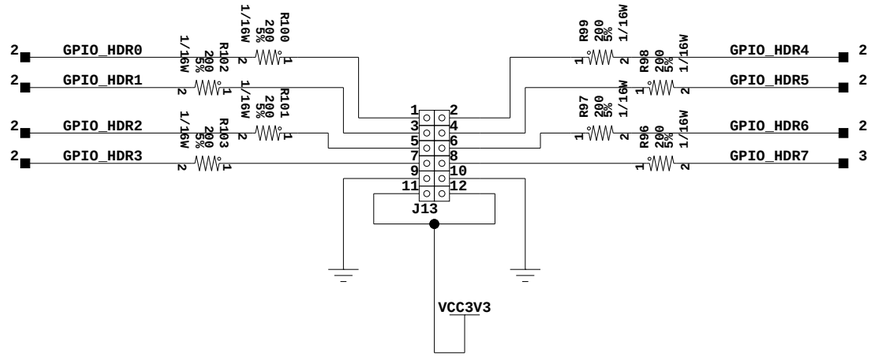


Fiducials

CP2103 USB Self-Powered

(26mA max)

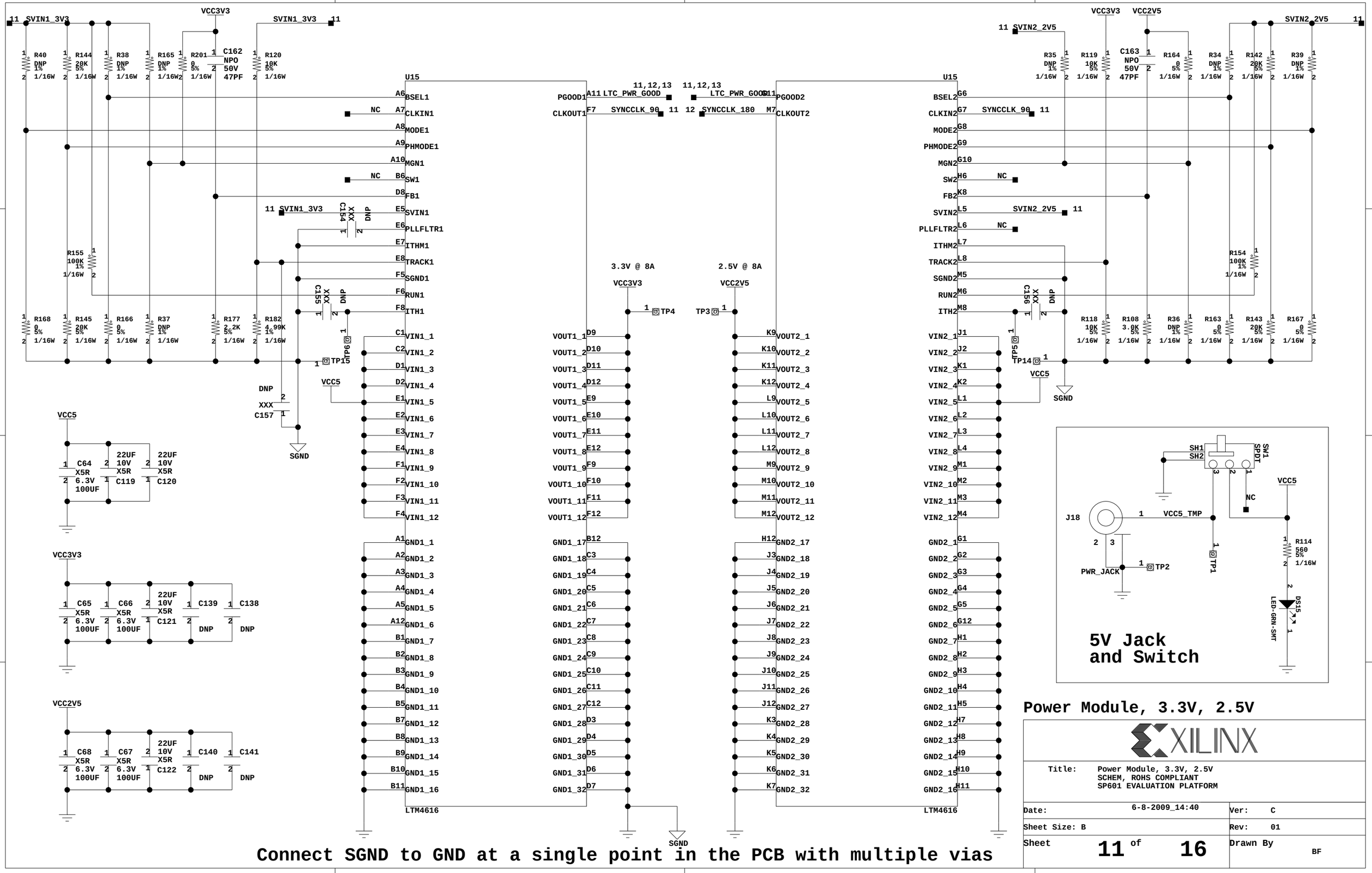


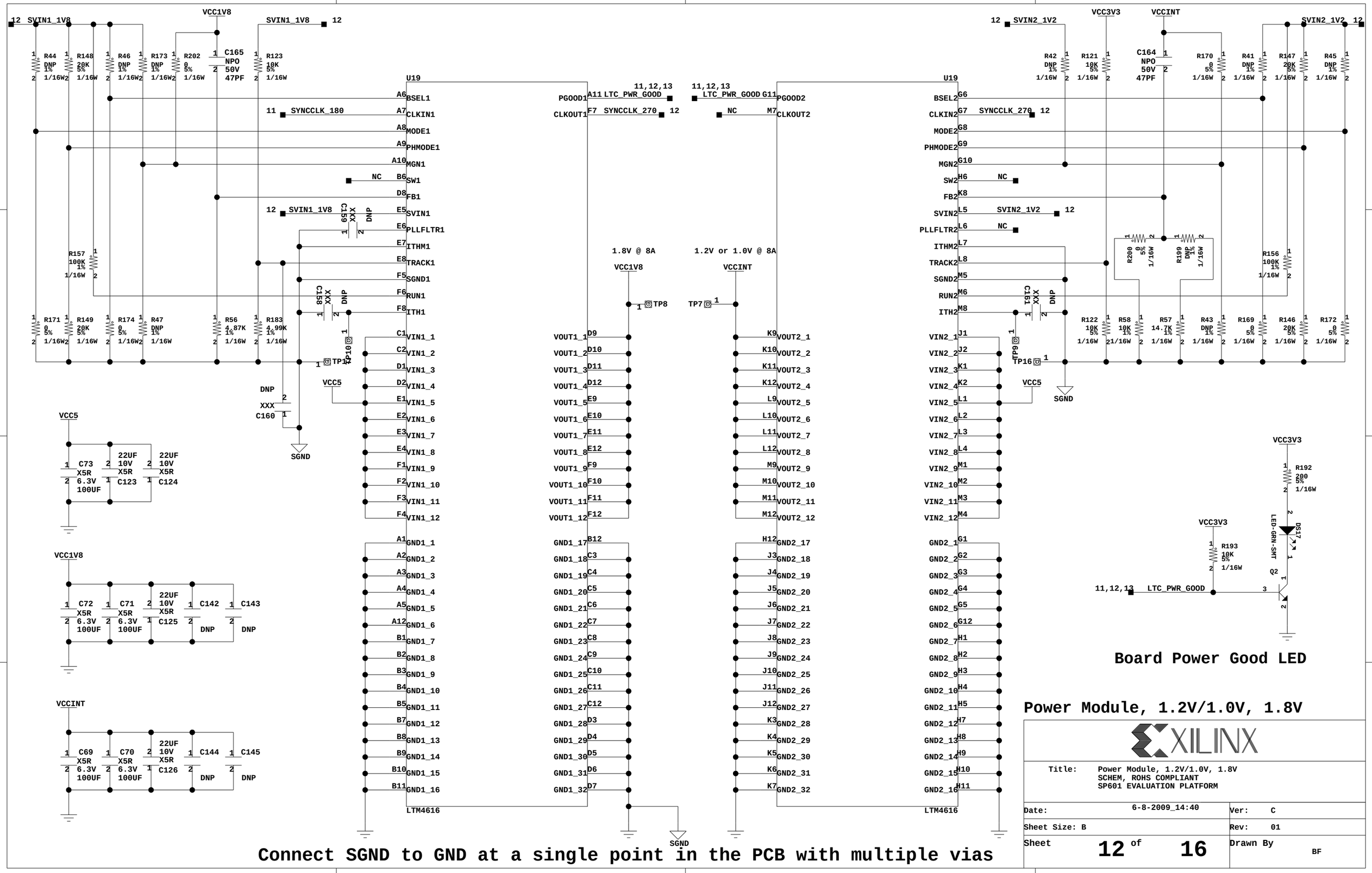


UART, IIC Header/EEPROM, GPIO Headers

The VIO voltage must match the appropriate bank IO voltage

Title:	UART, IIC Header/EEPROM, GPIO Headers SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM		
Date:	6-8-2009_14:40	Ver:	C
Sheet Size: B		Rev:	01
Sheet	10 of 16	Drawn By	BF


11 SVIN1_3V3
VCC3V3
SVIN1_3V3 11
R40 DNP 1% 1/16W
R144 20K 5% 1/16W
R38 DNP 1% 1/16W
R165 DNP 1% 1/16W
R201 0 5% 1/16W
C162 NPO 50V 47PF
R120 10K 5% 1/16W
U15
A6 BSEL1
NC A7 CLKIN1
A8 MODE1
A9 PHMODE1
A10 MGN1
NC B6 SW1
D8 FB1
11 SVIN1_3V3
C154 XXX DNP
E5 SVIN1
E6 PLLFLTR1
E7 ITHM1
E8 TRACK1
F5 SGND1
C155 XXX DNP
F6 RUN1
F8 ITH1
R155 100K 1% 1/16W
R168 0 5% 1/16W
R145 20K 5% 1/16W
R166 0 5% 1/16W
R37 DNP 1% 1/16W
R177 2.2K 5% 1/16W
R182 4.99K 1% 1/16W
TP6
TP15
C1 VIN1_1
C2 VIN1_2
D1 VIN1_3
D2 VIN1_4
E1 VIN1_5
E2 VIN1_6
E3 VIN1_7
E4 VIN1_8
F1 VIN1_9
F2 VIN1_10
F3 VIN1_11
F4 VIN1_12
VCC5
DNP
XXX
C157
SGND
VCC5
C64 X5R 6.3V 100UF
22UF 10V X5R C119
22UF 10V X5R C120
VCC3V3
C65 X5R 6.3V 100UF
C66 X5R 6.3V 100UF
22UF 10V X5R C121
C139 DNP
C138 DNP
VCC2V5
C68 X5R 6.3V 100UF
C67 X5R 6.3V 100UF
22UF 10V X5R C122
C140 DNP
C141 DNP
11,12,13 LTC_PWR_GOOD
PGOOD1 A11
CLKOUT1 F7 SYNCCLK_90 11
3.3V @ 8A
VCC3V3
TP4
VOUT1_1 D9
VOUT1_2 D10
VOUT1_3 D11
VOUT1_4 D12
VOUT1_5 E9
VOUT1_6 E10
VOUT1_7 E11
VOUT1_8 E12
VOUT1_9 F9
VOUT1_10 F10
VOUT1_11 F11
VOUT1_12 F12
GND1_1 A1
GND1_2 A2
GND1_3 A3
GND1_4 A4
GND1_5 A5
GND1_6 A12
GND1_7 B1
GND1_8 B2
GND1_9 B3
GND1_10 B4
GND1_11 B5
GND1_12 B7
GND1_13 B8
GND1_14 B9
GND1_15 B10
GND1_16 B11
GND1_17 B12
GND1_18 C3
GND1_19 C4
GND1_20 C5
GND1_21 C6
GND1_22 C7
GND1_23 C8
GND1_24 C9
GND1_25 C10
GND1_26 C11
GND1_27 C12
GND1_28 D3
GND1_29 D4
GND1_30 D5
GND1_31 D6
GND1_32 D7
LTM4616
SGND
11,12,13 LTC_PWR_GOOD
12 SYNCCLK_180 M7 CLKOUT2
2.5V @ 8A
VCC2V5
TP3
K9 VOUT2_1
K10 VOUT2_2
K11 VOUT2_3
K12 VOUT2_4
L9 VOUT2_5
L10 VOUT2_6
L11 VOUT2_7
L12 VOUT2_8
M9 VOUT2_9
M10 VOUT2_10
M11 VOUT2_11
M12 VOUT2_12
H12 GND2_17
J3 GND2_18
J4 GND2_19
J5 GND2_20
J6 GND2_21
J7 GND2_22
J8 GND2_23
J9 GND2_24
J10 GND2_25
J11 GND2_26
J12 GND2_27
K3 GND2_28
K4 GND2_29
K5 GND2_30
K6 GND2_31
K7 GND2_32
LTM4616
VCC3V3
VCC2V5
11 SVIN2_2V5
SVIN2_2V5 11
R35 DNP 1% 1/16W
R119 10K 5% 1/16W
C163 NPO 50V 47PF
R164 0 5% 1/16W
R34 DNP 1% 1/16W
R142 20K 5% 1/16W
R39 DNP 1% 1/16W
U15
BSEL2 G6
CLKIN2 G7 SYNCCLK_90 11
MODE2 G8
PHMODE2 G9
MGN2 G10
SW2 H6 NC
FB2 K8
SVIN2 L5 SVIN2_2V5 11
PLLFLTR2 L6 NC
ITHM2 L7
TRACK2 L8
SGND2 M5
C156 XXX DNP
RUN2 M6
ITH2 M8
R154 100K 1% 1/16W
R118 10K 5% 1/16W
R108 3.0K 5% 1/16W
R36 DNP 1% 1/16W
R163 0 5% 1/16W
R143 20K 5% 1/16W
R167 0 5% 1/16W
TP5
TP14
VCC5
SGND
VIN2_1 J1
VIN2_2 J2
VIN2_3 K1
VIN2_4 K2
VIN2_5 L1
VIN2_6 L2
VIN2_7 L3
VIN2_8 L4
VIN2_9 M1
VIN2_10 M2
VIN2_11 M3
VIN2_12 M4
GND2_1 G1
GND2_2 G2
GND2_3 G3
GND2_4 G4
GND2_5 G5
GND2_6 G12
GND2_7 H1
GND2_8 H2
GND2_9 H3
GND2_10 H4
GND2_11 H5
GND2_12 H7
GND2_13 H8
GND2_14 H9
GND2_15 H10
GND2_16 H11
LTM4616
SH1
SH2
SW1 SPDT
VCC5
NC
J18
VCC5_TMP
R114 560 5% 1/16W
PWR_JACK
TP2
TP1
DS15 LED-GRN-SMT
5V Jack and Switch
Power Module, 3.3V, 2.5V
XILINX
Title: Power Module, 3.3V, 2.5V
SCHEM, ROHS COMPLIANT
SP601 EVALUATION PLATFORM
Date: 6-8-2009_14:40
Ver: C
Sheet Size: B
Rev: 01
Sheet 11 of 16
Drawn By BF
Connect SGND to GND at a single point in the PCB with multiple vias


12 SVIN1_1V8
VCC1V8
SVIN1_1V8 12
R44 DNP 1% 1/16W
R148 20K 5% 1/16W
R46 DNP 1% 1/16W
R173 DNP 1% 1/16W
R202 0 5% 1/16W
C165 NPO 50V 47PF
R123 10K 5% 1/16W
U19
A6 BSEL1
11 SYNCCLK_180
A7 CLKIN1
A8 MODE1
A9 PHMODE1
A10 MGN1
NC B6 SW1
D8 FB1
12 SVIN1_1V8
C159 XXX DNP
E5 SVIN1
E6 PLLFLTR1
E7 ITHM1
E8 TRACK1
F5 SGND1
C158 XXX DNP
F6 RUN1
F8 ITH1
TP10
TP1
C1 VIN1_1
C2 VIN1_2
D1 VIN1_3
D2 VIN1_4
E1 VIN1_5
E2 VIN1_6
E3 VIN1_7
E4 VIN1_8
F1 VIN1_9
F2 VIN1_10
F3 VIN1_11
F4 VIN1_12
R157 100K 1% 1/16W
R171 0 5% 1/16W
R149 20K 5% 1/16W
R174 0 5% 1/16W
R47 DNP 1% 1/16W
R56 4.87K 1% 1/16W
R183 4.99K 1% 1/16W
VCC5
DNP
XXX
C160
SGND
VCC5
C73 X5R 6.3V 100UF
22UF 10V X5R C123
22UF 10V X5R C124
VCC1V8
C72 X5R 6.3V 100UF
C71 X5R 6.3V 100UF
22UF 10V X5R C125
C142 DNP
C143 DNP
VCCINT
C69 X5R 6.3V 100UF
C70 X5R 6.3V 100UF
22UF 10V X5R C126
C144 DNP
C145 DNP
11,12,13 LTC_PWR_GOOD
PGOOD1 A11
CLKOUT1 F7 SYNCCLK_270 12
1.8V @ 8A
VCC1V8
TP8
VOUT1_1 D9
VOUT1_2 D10
VOUT1_3 D11
VOUT1_4 D12
VOUT1_5 E9
VOUT1_6 E10
VOUT1_7 E11
VOUT1_8 E12
VOUT1_9 F9
VOUT1_10 F10
VOUT1_11 F11
VOUT1_12 F12
GND1_1 A1
GND1_2 A2
GND1_3 A3
GND1_4 A4
GND1_5 A5
GND1_6 A12
GND1_7 B1
GND1_8 B2
GND1_9 B3
GND1_10 B4
GND1_11 B5
GND1_12 B7
GND1_13 B8
GND1_14 B9
GND1_15 B10
GND1_16 B11
GND1_17 B12
GND1_18 C3
GND1_19 C4
GND1_20 C5
GND1_21 C6
GND1_22 C7
GND1_23 C8
GND1_24 C9
GND1_25 C10
GND1_26 C11
GND1_27 C12
GND1_28 D3
GND1_29 D4
GND1_30 D5
GND1_31 D6
GND1_32 D7
LTM4616
SGND
11,12,13 LTC_PWR_GOOD G11
PGOOD2
NC M7
CLKOUT2
1.2V or 1.0V @ 8A
VCCINT
TP7
K9 VOUT2_1
K10 VOUT2_2
K11 VOUT2_3
K12 VOUT2_4
L9 VOUT2_5
L10 VOUT2_6
L11 VOUT2_7
L12 VOUT2_8
M9 VOUT2_9
M10 VOUT2_10
M11 VOUT2_11
M12 VOUT2_12
H12 GND2_17
J3 GND2_18
J4 GND2_19
J5 GND2_20
J6 GND2_21
J7 GND2_22
J8 GND2_23
J9 GND2_24
J10 GND2_25
J11 GND2_26
J12 GND2_27
K3 GND2_28
K4 GND2_29
K5 GND2_30
K6 GND2_31
K7 GND2_32
LTM4616
12 SVIN2_1V2
VCC3V3
VCCINT
SVIN2_1V2 12
R42 DNP 1% 1/16W
R121 10K 5% 1/16W
C164 NPO 50V 47PF
R170 0 5% 1/16W
R41 DNP 1% 1/16W
R147 20K 5% 1/16W
R45 DNP 1% 1/16W
U19
BSEL2 G6
CLKIN2 G7 SYNCCLK_270 12
MODE2 G8
PHMODE2 G9
MGN2 G10
SW2 H6 NC
FB2 K8
SVIN2 L5 SVIN2_1V2 12
PLLFLTR2 L6 NC
ITHM2 L7
TRACK2 L8
SGND2 M5
RUN2 M6
C161 XXX DNP
ITH2 M8
TP9
TP16
VIN2_1 J1
VIN2_2 J2
VIN2_3 K1
VIN2_4 K2
VIN2_5 L1
VIN2_6 L2
VIN2_7 L3
VIN2_8 L4
VIN2_9 M1
VIN2_10 M2
VIN2_11 M3
VIN2_12 M4
VCC5
SGND
R200 0 5% 1/16W
R199 DNP 1% 1/16W
R156 100K 1% 1/16W
R122 10K 5% 1/16W
R58 10K 1% 1/16W
R57 14.7K 1% 1/16W
R43 DNP 1% 1/16W
R169 0 5% 1/16W
R146 20K 5% 1/16W
R172 0 5% 1/16W
GND2_1 G1
GND2_2 G2
GND2_3 G3
GND2_4 G4
GND2_5 G5
GND2_6 G12
GND2_7 H1
GND2_8 H2
GND2_9 H3
GND2_10 H4
GND2_11 H5
GND2_12 H7
GND2_13 H8
GND2_14 H9
GND2_15 H10
GND2_16 H11
LTM4616
VCC3V3
R192 200 5% 1/16W
DS17 LED-GRN-SMT
VCC3V3
R193 10K 5% 1/16W
Q2
11,12,13 LTC_PWR_GOOD
Board Power Good LED
Power Module, 1.2V/1.0V, 1.8V
XILINX
Title: Power Module, 1.2V/1.0V, 1.8V
SCHEM, ROHS COMPLIANT
SP601 EVALUATION PLATFORM
Date: 6-8-2009_14:40
Ver: C
Sheet Size: B
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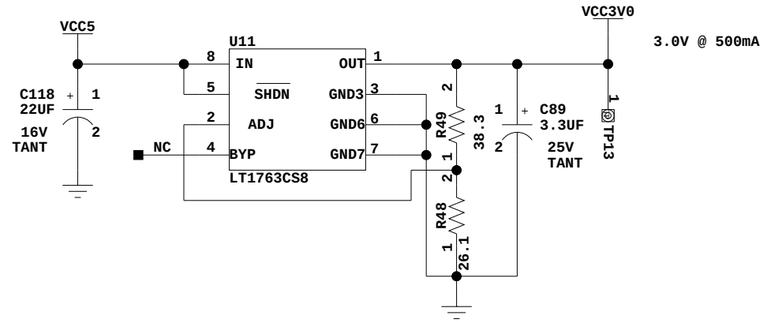
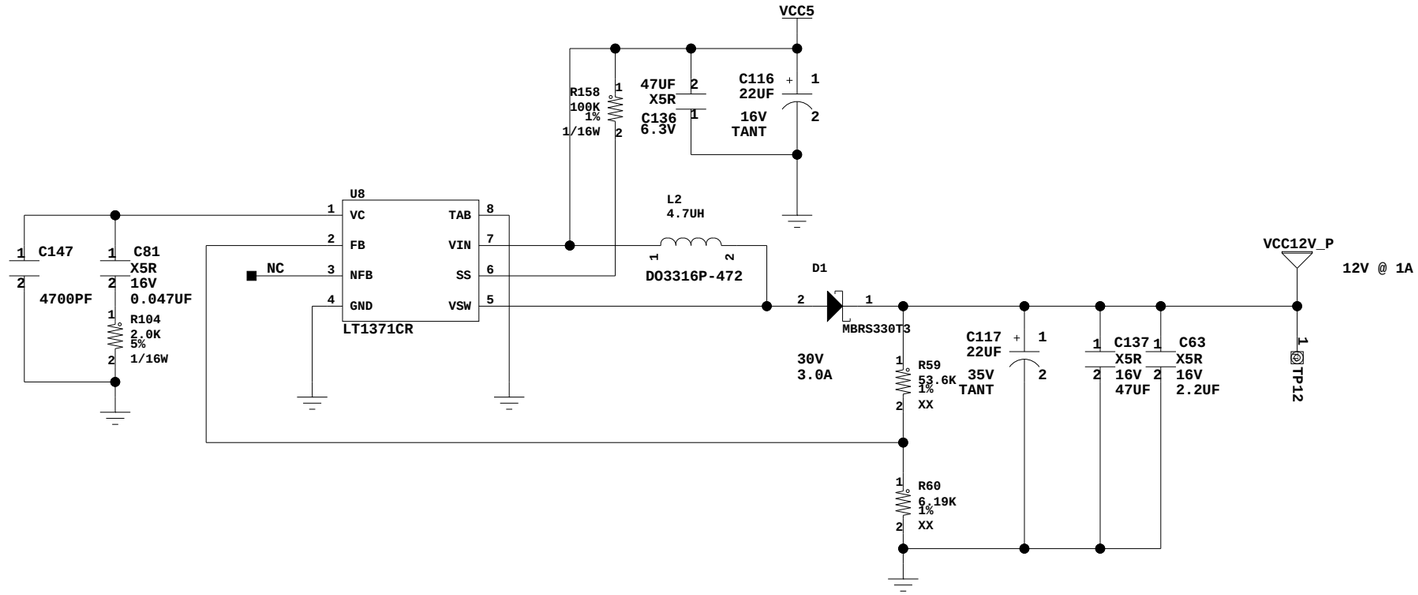
Sheet 12 of 16
Drawn By BF
Connect SGND to GND at a single point in the PCB with multiple vias





Power Supplies, 12V, 3.0V, 0.9V

Title:	Power Supplies, 12V, 3.0V, 0.9V SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM		
Date:	6-23-2009_14:57	Ver:	C
Sheet Size: B		Rev:	01
Sheet	13 of 16	Drawn By	BF

The Embedded USB JTAG Download circuit on this page is for reference only!
This circuit should not be designed into an end customer product or solution.
Xilinx will not provide support on this embedded USB JTAG Download circuit.

U12

PART_NUMBER=CY7C68013A

USB CONTROLLER

U9

PART_NUMBER=XC2C256

PARALLEL TO SERIAL CONVERTER

USB CONNECTOR

USB TYPE B RECEPTACLE

NOTE: EMBEDDED VERSION IS NOT BUS POWERED

TARGET INTERFACE CONNNECTIONS	
FROM	TO JTAG
FPGA_TCK	TCK ALL DEVICES
FPGA_TMS	TMS ALL DEVICES
USB_HEADER_TDI	FIRST DEVICE TDI
JTAG_TDO	LAST DEVICE TDO
EMBEDDED_INIT	NO CONNECTION

3.3V INTERFACE TO LOCAL JTAG OR SLAVE-SERIAL DEVICE CHAIN.
FOR LONG CHAINS OR TRACES, DISTRIBUTE EMBEDDED_TCK
AND EMBEDDED_TMS WITH LVDS BUFFERS.

LEGEND:

- (01) OPTIONAL NETS ROUTED IN PARALLEL TO LOCAL 2MM CABEL CONNECTOR J1.
- ● COMPONENTS TO BE LOADED FOR THE PRODUCTION ASSEMBLY VERSION ONLY.
- ● OPTIONAL COMPONENTS THAT SUPPORT DEBUG AND/OR DIAGNOSTICS.

NOTE:

MAKE PARALLEL CONNECTIONS TO J1 (OPTION B) AT EACH OF THE NETS MARKED (01) TO FACILITATE FASTER IN-CIRCUIT RE-PROGRAMMING OF THE CPLD DURING BOARD TEST.
J1 DOES NOT NEED TO BE PROGRAMMED DURING PRODUCTION, BUT THE ASSEMBLY FOOTPRINT IS RECOMMENDED FOR THE PWB LAYOUT.

Embedded USB JTAG: USB Controller, CPLD

Drawing Number: 0381242	
Date: 14-JUNE-2006	Ver: C
Sheet Size: D	Rev: 01
Sheet 14 of 16	Drawn By SCHWEIGLER

LAST REVISION: 6-23-2009_12:13

The Embedded USB JTAG Download circuit on this page is for reference only!
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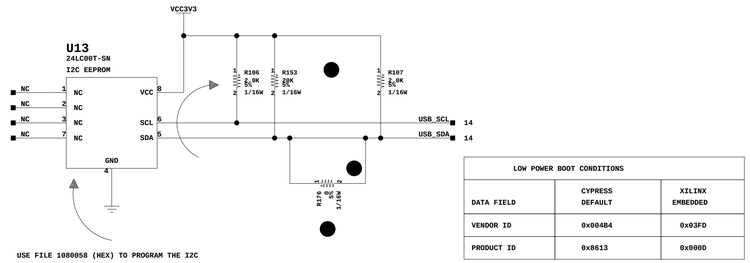
Xilinx will not provide support on this embedded USB JTAG Download circuit.

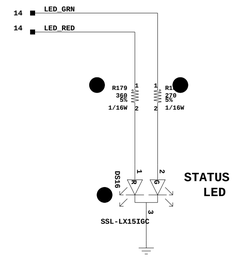
DEFAULT PID/VID EEPROM



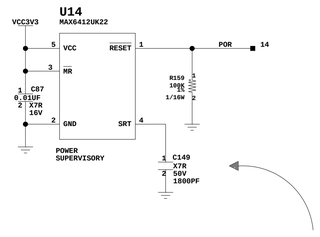
USE FILE 10800S8 (HEX) TO PROGRAM THE I2C PROM PRIOR TO ASSEMBLY.

LOW POWER BOOT CONDITIONS		
DATA FIELD	CYPRESS DEFAULT	XILINX EMBEDDED
VENDOR ID	0x004B4	0x03FD
PRODUCT ID	0x8613	0x000D

STATUS LEDS (OPTION A)

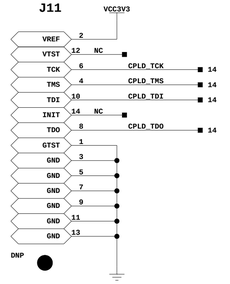


POWER-ON RESET

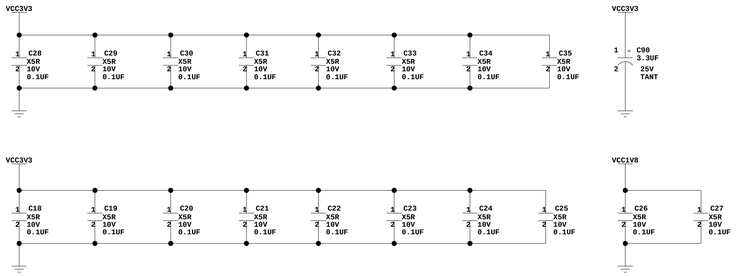


NOTE: PRODUCES 5MS POWER-ON RESET

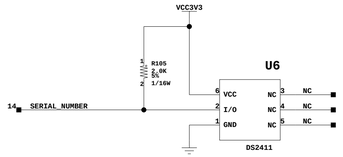
PC4 JTAG CONNECTOR (OPTION B)



BYPASS CAPACITORS



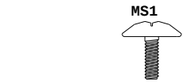
ELECTRONIC SERIAL NUMBER



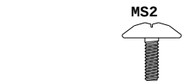
Embedded USB JTAG: IIC, POR, Decoupling, LED, JTAG Header, Serial Number

Drawing Number: 0381242	
Date: 14-JUNE-2006	Ver: C
Sheet Size: D	Rev: 01
Sheet 15 of 16	Drawn By SCHWEIGLER

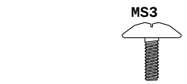
LAST REVISION: 6-23-2009_12:13



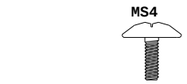
MACHINE_SCREW_SS_PHILHD_4-40_X_3-8



MACHINE_SCREW_SS_PHILHD_4-40_X_3-8



MACHINE_SCREW_SS_PHILHD_4-40_X_3-8



MACHINE_SCREW_SS_PHILHD_4-40_X_3-8

NUT_SS_4-40

NUT_SS_4-40

NUT_SS_4-40

NUT_SS_4-40

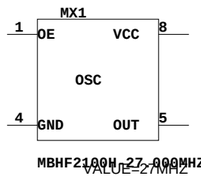
RUBBER_BUMPER

RUBBER_BUMPER

RUBBER_BUMPER

RUBBER_BUMPER

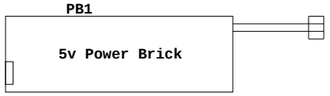
USB Mini-B Cable



Half Size Oscillator

JUMPER_BLOCK_2-PIN

JUMPER_BLOCK_2-PIN



Mechanical Components

XILINX

Title:	Mechanical Components SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM		
Date:	6-8-2009_14:50	Ver:	C
Sheet Size: B		Rev:	01
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