Analog Front End Integrated Circuit for 13.56MHz RFID Base Station

General Description

The EM4094 is an analogue front end for 13.56MHz RFID reader systems. It is highly versatile so it can be used in different reader systems having sub carrier frequencies from 212kHz to 848kHz, hence covering ISO14443 and ISO15693 standards.
The adaptability is achieved using a 3 wire serial interface to program the system option bits.
The EM4094 operating voltage is comprised between 3.3V and 5V.
The push-pull transmitter generates 200mW output RF power into a 50Ω load. The output stage drivers are capable of OOK or ASK modulation from 7% up to 30% of AM modulation.
The EM4094 reader chip is available in SO16, TSSOP16, TSSOP20 and SO20 package.

Applications

- Low cost reader modules
- Hand held reader

Features

- ISO15693 & ISO14443 type A, B and C standard compatibility
- HF EPC compliant
- Supports EM4006 read only transponder IC
- 3.3V or 5V Power Supply (analogue and digital)
- Antenna driver using OOK or ASK modulation, single or double antenna drivers
- ASK modulation index adjustable from 7% up to 30%
- High output RF power of 200mW from 5V supply
- Antenna short circuit protection
- Multiple receiver input for high communication reliability
- 848KHz BPSK internal decoder (ISO14443 type B)
- Multiple sub-carrier receiving compatibility (212kHz, 424kHz and 848kHz)
- Multiple sub-carrier coding compatibility (Manchester, Miller, BPSK)
- Built-in receive low-pass filter which cut-off frequencies are selectable between 400kHz and 1MHz
- Built-in receive high-pass filter cut-off frequency selectable between 100kHz, 200kHz and 300kHz
- Selectable receive gain from 0dB up to 40dB
- Serial 3 pins interface for option selection
- Power down mode controlled by the 3 wires SPI
- Output Power: 200mW for SO20w and TSSOP-20
  100mW for SO16w and TSSOP16
- Operation temperature range -40°C to +85°C

Typical Application

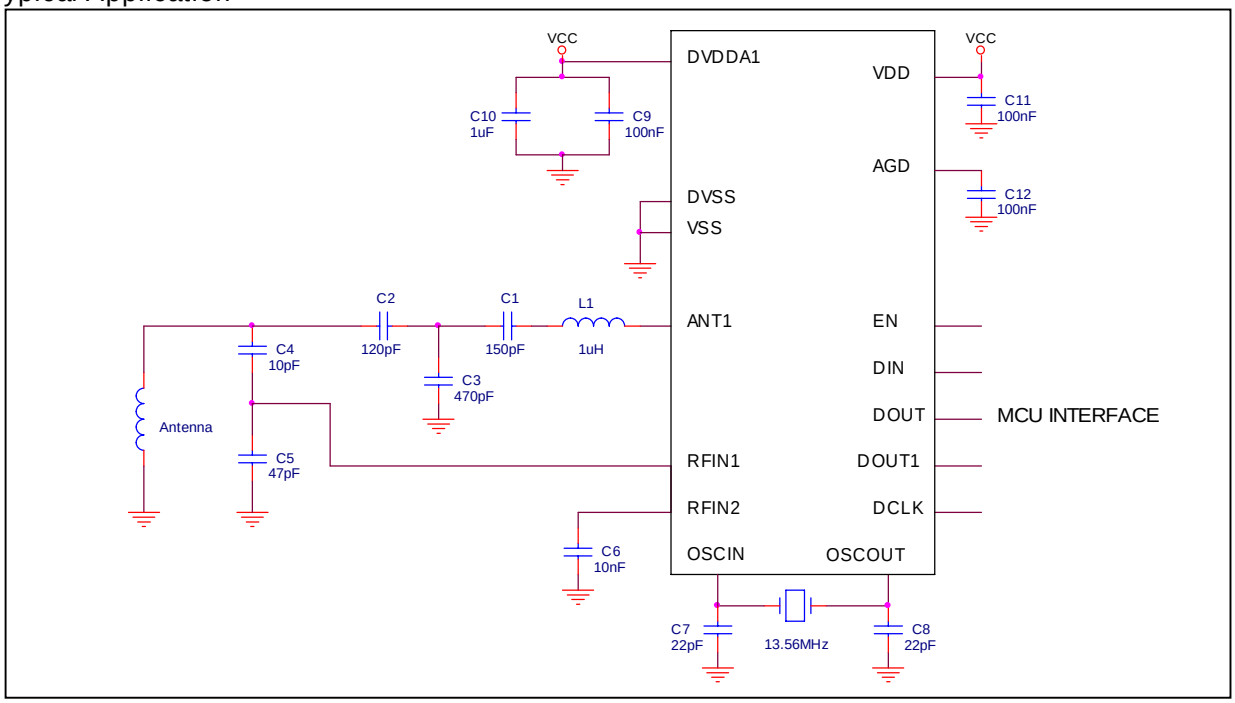

Figure 1

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1. Block Diagram

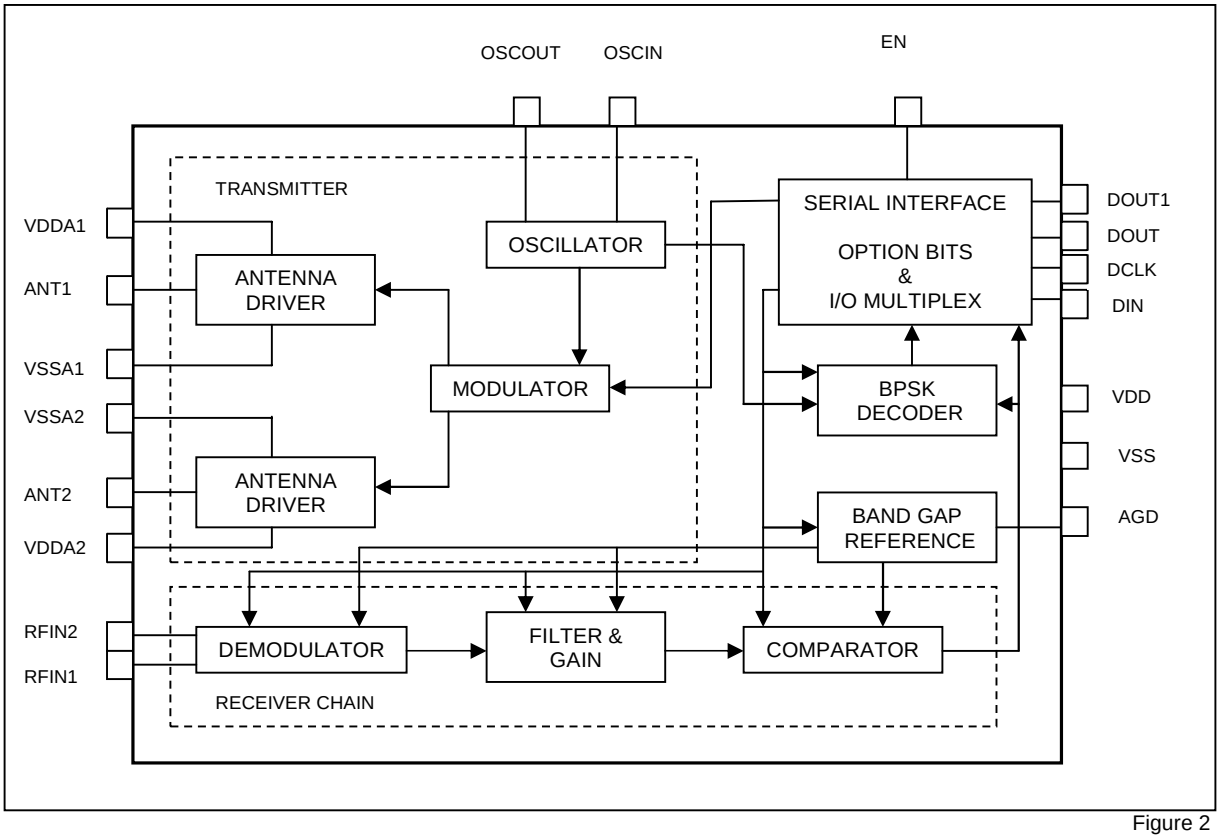


Figure 2

2. Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

3. Absolute Maximum Ratings

3.1 Absolute Maximum Ratings

V_{SS} = 0V

Parameters	Symbol	Conditions
Maximum voltage at VDD	V_{VDDMAX}	V_{VSS}+6V
Minimum voltage at VDD	V_{VDDMIN}	V_{VSS}-0.3V
Max. voltage other pads	V_{MAX}	V_{VDD}+0.3V
Min. voltage other pads	V_{MIN}	V_{VSS}-0.3V
Max. junction temperature	T_{JMAX}	+125°C
Storage temperature range	T_{STO}	-50 to +150°C
Electrostatic discharge max. to MIL-STD-883 method 3015 ref VSS	V_{ESD}	2KV
Electrostatic discharge max. to MIL-STD-883 method 3015 for pins ANT1 & ANT2	V_{ESDANT}	4KV
Maximum Input / Output current on all pads except VDD, VDDA1, VDDA2, VSS, VSSA1, VSSA2, ANT1 and ANT2	I_{IMAX} I_{OMAX}	10mA
Maximum AC peak current on VDDA1, VDDA2, VSSA1, VSSA2, ANT1 and ANT2 pads at 13MHz, duty cycle 50% (per antenna driver)	I_{ANTMAX}	100mA

Table 1

Stresses above these listed maximum ratings may cause permanent damages to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operation section of this specification is not implied. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

3.2 Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units
Power supply voltage	V_{VDD}	4.5	5	5.5	V
Operating junction temperature	T_J	-40		+110	°C
Package Thermal resistor for SO16W (note 1)	R_{thJ-A}		65		°C/W
Package Thermal resistor for TSSOP16 (note1)	R_{thJ-A}		89		°C/W
Package Thermal resistor for SO20W (note 1)	R_{thJ-A}		55		°C/W
Package Thermal resistor for TSSO20 (note 1)	R_{thJ-A}		73.2		°C/W
Load impedance on ANT1 or ANT2 output drivers	Z_{ANT}	(7+j0) Ω			
Quartz load capacitors (note 2)	C1 & C2	2 x 22pF			
Capacitors VDDA1, VSSA1 filtering (note 2)	C7, C8 & C10	1nF, 100nF and 10µF connected in parallel			
Capacitors VDDA2, VSSA2 filtering (note 2)	C5, C6 & C9	1nF, 100nF and 10µF connected in parallel			
Capacitors VDD, VSS filtering (note 2)	C11 & C12	1nF, 100nF connected in parallel			
AGD filtering capacitors (note 2)	C13	100nF (optional 1nF in parallel)			

Table 2

Note 1: No fan convection, reader chip mounted on a multi layer PCB.
The maximum operating temperature is calculated with the following formula:

$$T_a = (RTH_{ja} * P) - T_{jmax}$$

T_j: maximum junction temperature, T_a: ambient temperature

Note 2:

- For the capacitors, refer to the Typical Application schematic on the first page of the datasheet.
- The Quartz load capacitors are in COG ceramic technology (±5%)
- Use COG ceramic technology (±5%) for the 1nF capacitors.
- Use X7R ceramic technology (±10%) for the 100nF capacitors.
- Use tantalum electrolytic technology for the 10µF capacitors.

The package thermal resistors are based on a multi-layer test board and zero airflow. The package performance is highly dependent on board and environmental conditions.

3.3 Electrical Characteristics

Unless otherwise specified: $V_{VSS} = V_{VSSA1} = V_{VSSA2} = 0V$ & $V_{VDD} = V_{VDDA1} = V_{VDDA2} = 5V$, T_J= -40 to +110°C.

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
General DC parameters						
Supply current in power-down mode	I_{PD}			1	5	µA
Supply current excluding antenna driver current	I_{ON}	Option bits value: 04800001 (Hexa)		12	20	mA
AGD level	V_{AGD}		2.3	2.5	2.7	V
Power on reset level	V_{POR}		1.4	2.1	3.6	V
Antenna Drivers						
ANT1 (or ANT2) driver output impedance	R_{AD}	I_{ANT} = 100mA 100% modulation index	3	7	12	Ω
ANT1 (or ANT2) driver output impedance	R_{AD}	I_{ANT} = 100mA 10% modulation index	5	10	15	Ω
Serial Interface						
Input logic low	V_{IL}				$0.2V_{DD}$	V
Input logic high	V_{IH}		$0.8V_{DD}$			V
Output logic high	V_{OH}	I_{SOURCE} = 1mA	$0.9V_{DD}$			V
Output logic low	V_{OL}	I_{SINK} = 1mA			$0.1V_{DD}$	V
Maximum serial interface clock frequency	F_{max}				1	MHz
AM demodulation						
RF amplitude at RFIN inputs	V_{RFIN}		2.5		V_{VDD}	V_{PP}
RFIN input resistance	R_{RFIN}		5	10	20	kΩ
Receiver sensitivity @ 212kHz		(note 3)		1.5	3	mV_{pp}
Receiver sensitivity @ 424kHz		(note 3)		2.2	4.5	mV_{pp}
Receiver sensitivity @ 848kHz	V_{SENS}	(note 3)		3.5	6	mV_{pp}

Table 3

Note 3: Sine wave envelope, max. gain, RF amplitude in V_{RFIN}

3.4 Timing Characteristics

Unless otherwise specified: $V_{VSS} = V_{VSSA1} = V_{VSSA2} = 0V$ & $V_{VDD} = V_{VDDA1} = V_{VDDA2} = 5V$, T_J= -40 to +110°C.

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Xtal Oscillator						
Transconductance	gm	Normal mode (note 4)	0.3	0.9	1.6	mS
		Hi oscillator mode (note 4)	1.5	2.7	4.0	mS
Set-up time after power down	T_{set}			5	15	Ms
AM demodulation						
Recovery time of reception after antenna modulation	T_{rec}				100	µs

Table 4

Note 4: It is recommended to use the high gm transconductance.
Crystal electrical parameters:

- Quality factor min: 26000
- Series resistance typ: 20Ω
- Static capacitance typ: 2.8pF

4. Functional Description

The EM4094 Analog Front End can be adapted to any kind of reader system using the 31 option bits.
The option bits chapter gives a global view and specifies all of the reader chip options.

4.1 Power Supply (VDD & VSS)

The EM4094 analogue front end can operate at 3.3V or 5V. The power supply voltage has to be the same on the analogue and digital input lines (VDD, VDDA1, VDDA2).
It is strongly recommended to use a regulated supply. Power supply ripples and noise, inside the receiver frequency range, degrades the overall system performances.
To use the EM4094 at 3.3V, an external resistor has to be connected on the AGD output to fix a voltage of 2.0V on AGD. The external resistor can be switched off (using for example a microcontroller I/O) when the reader chip is not used.

4.2 Power management

There are two available power modes. The selection of these two modes is done with the Power up Flag (option bit 1).

There are two ways to put the EM4094 Analog Front End in a power down state:

- Reseting the power up flag.
- Applying a low level on EN input. In that case, only the analog circuitry goes to Power Down but the SPI interface remains active.

When EN is changed to high (and power up flag is high) the EM4094 goes immediately to the mode in which it was before EN went low level.

In power-up mode, the oscillator is started followed by the transmitter and the receiver. When the chip is ready to operate (quartz oscillator, receiver operating points are ready and transmitter is not shorted (if bit 5 is set) a 100µs ready pulse is generated on DOUT pin.

After that condition, the chip goes to normal operation mode. DOUT corresponds to the demodulated signal output and DOUT1 is the 13.56MHz-clock output (if DOUT1 is not used as BPSK clock output in ISO14443 type B standard).

4.3 Driver Power Supply (VDDA1, VSSA1 & VDDA2, VSSA2)

Supply lines should be separately filtered for analogue chip supply and antenna driver supplies.

Any variations in supply voltage directly modulate the antenna driver and they are fed to the receiver's input. The power supply sensitivity range, for frequency components which are in the receiving bandwidth, is the same as the RFIN sensitivity.

4.4 Band-Gap reference

The reference voltage (2.5V) is generated internally by a Band-gap reference and uses an external capacitor for blocking.

4.5 Internal Oscillator

The oscillator is driven by the13.56MHz external crystal to generate the RF frequency. The external quartz crystal is connected to the load capacitors as indicated in Figure 1.

It is also possible to apply an external clock source, DC coupled to OSCIN, according to Vi input levels, to drive the internal oscillator.
When option bit 27 is set, OSCIN corresponds to the digital input of the internal oscillator.
The oscillator start-up time can be decreased by setting option bit 26 (oscillator gain).

4.6 Antenna drivers

The antenna driver produces the RF signal from the oscillator output. The PMOS and NMOS driver side are fed by non-overlapping signals (3ns) to minimize the power consumption.
The output resistance of each antenna driver is typically 7Ω. It is changed, during the field modulation, to set the right ASK modulation index level (option bits 2, 3, 4).
The two integrated antenna drivers can be used in three possible configurations depending on the output power level (refer to application chapter on page 11).
When a single driver configuration is selected, the output power level on the 50Ω load is 100mW.
For a 200mW output power, both drivers have to be used in parallel configuration to double the output power (option bit 6).

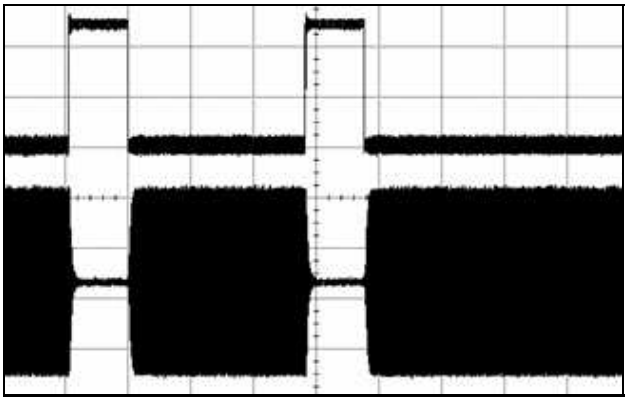
The drivers can operate in push-pull configuration (option bit 7). This mode can be used in case of direct antenna connection. In that configuration, the reader antenna is connected to the output drivers through a resonant capacitor (LC tank adjusted to 13.56MHz)
Take note that, in direct antenna configuration, the output power can exceed 200mW. Chip cooling requirements must be carefully considered.
To be compliant with national country regulations, it could be necessary to add a filtering structure between the IC output stage drivers and the antenna. For more information, please, refer to the product application note.
The short protection circuit (option bit 5) prevents damage to the output driver when the ANT pin is shorted to ground or to the power supply.

4.7 Modulator

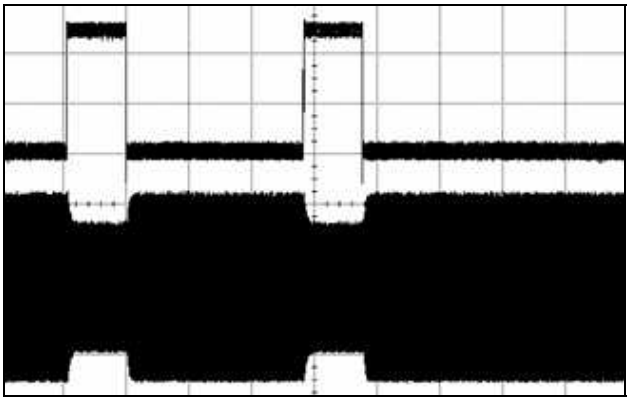
The modulator enables OOK or ASK modulation of the RF signal on the antenna outputs (ANT1 and ANT2).

When the device is in normal mode, DIN corresponds to the modulator input.

A high input level, on DIN input, causes a low field (ASK modulation index) or a field-stop if OOK modulation is chosen.



Upper trace: digital input (DIN) modulation input
Lower trace: transmitted field on ANT1 for ie
Reader modulation is set to OOK (100% AM)



Upper trace: digital input (DIN) modulation input
Lower trace: transmitted field on ANT1 for ie
Reader modulation is set to 16% ASK

The selection between OOK and ASK modulation depth is done using configuration bits 2, 3 and 4.

The field modulation index can be adjusted from 7% up to 30% covering all the ISO standard air interface requirements.

Before and after a modulation phase, the receiver input is disconnected from the antenna circuitry to preserve DC operating point setting.
For high quality factor systems, it may be necessary to prolong (option bit 25) the hold time after modulation to allow settling of the resonant circuit.

4.8 Receiver

The receiver senses the envelope of the signal present on the inputs RFIN1 or RFIN2 (option bit 14). These two inputs, used with external components, permit the detection of amplitude or phase modulated signals.

Any RF frequency components still present in the envelope signal are removed by a second order low pass filter.
The received signal DC component is removed by the high pass filter, which has selectable corner frequency (option bits 8 and 9).
The signal is amplified and further processed by the low pass filtering stage, which corner frequency is selectable (option bit 10).
The gain selection (option bits 11, 12 and 13) should be chosen according to the reader system parameters.

Modifying the signal bandwidth changes noise level and results in different input sensitivity.

These three bits define 8 gain settings according to the option bit table. The total gain range is 40dB.

The output signal, in normal mode, can be a digitized sub-carrier, a 106kbit/s BPSK decoded bit stream (DOUT) or an analogue output used for DSP decoding (DOUT1).

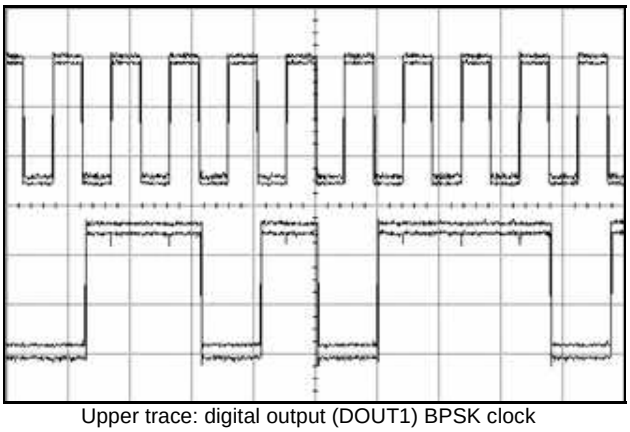
When a direct sub-carrier signal is selected, the tag answer is displayed on the DOUT pin. In such configuration, DOUT1 corresponds to the 13.56MHz clock output, which can be used for synchronization of an external micro-controller used for decoding.

4.9 BPSK Decoder

The internal BPSK decoder is designed to decode the transponder's sub-carrier signal according to the ISO14443-type B coding procedure described in the ISO 14443-B standard.

First 80 pulses are used as start of frame. The initial Phase State of the sub-carrier is defined as logical "1" and the first phase transition represents a change from logical "1" to logical "0". The sub-carrier frequency is 13.56MHz divided by 16 and each bit period consists of 8 pulses according to ISO14443-B standard.

The BPSK decoder is enabled by setting to a high level option bit 22. When this option bit is set, the decoded bit-stream is available on pin DOUT and the bit clock on pin DOUT1. The data is valid on the rising edge of bit clock.



Upper trace: digital output (DOUT1) BPSK clock
Bottom trace: digital output (DOUT) BPSK decoded data

The BPSK decoder decodes the transponder's signal, which can have a frequency offset. The transponders clock extractor can omit or add some clock transitions at modulation.
Successful operation, in such conditions, requires a frequency adaptive decoder. When option bit 23 is set, the decoder measures the average frequency of the 80 pulses (SOF) and adjusts the internal shift register to the appropriate length.
The decoder is capable of correct operation at incoming bit-stream frequencies of 847.5kHz +/-10%.

When the internal BPSK decoder is not activated and option bit 24 is set, DOUT1 corresponds to the output of the AGC amplifier.

4.10 AGC system

The integrated AGC system can be activated via option bit 15. The AGC amplifier has a 40dB gain correction depth.
The AGC system is adapted to all RFID communication protocols.
Before the transponder starts to emit the data, the receiver gain is set to maximum (option bits 11,12,13).
When the reader detects a transponder signal that is above the attack threshold the receiver gain is rapidly reduced (option bits 18 and19) to fit the signal into a linear range of the receiver.
The gain remains unchanged as long as the signal level is above the decay threshold.

When the received signal falls below the decay threshold for a period of time set by option bits 20 and 21, the reader logic establishes that the communication with one transponder is finished and makes a fast decay to return to the maximum gain.
The receiver is ready to demodulate the emission of the next transponder, which can be far away from the reader antenna. This feature is necessary for anti-collision purposes.

With transponders that have a modulation DC level shift significantly higher than modulation sub-carrier AC level, the AGC can react on DC shift and decrease the system gain too much.
It is possible not to attack the first pulse (option bit 16) in a burst (for OOK modulation) to allow the DC level to settle before AGC action. The time after which the first pulse in a burst is not attacked (shortest sub-carrier stop in OOK modulation is 1/10 of the time) is set by option bits 20, 21 as decay wait time. It is also possible to use slow decay mode (option bit 17). The slow decay is started when the received signal falls below the decay threshold. The decay rate is one gain step per time defined by option bits 20 and 21.
When AGC system is disabled the receiver gain is directly controlled by option bits 11, 12, 13

4.11 Serial Interface

The serial interface is used to control the EM4094 option bits setting.
A high level on DCLK and a rising edge on DIN reset the serial interface. After the reset, the DIN signal is shifted to the internal register on every rising edge on DCLK.

During first 31 DCLK transitions, the DIN data are read to the chip while during the 32nd transition the chip exits the SPI configuration mode and enters the normal mode.

In normal mode:

- DIN is used to modulate the field (high DIN: low reader filed for ASK or no field for OOK).
- DCLK must be low in normal mode.
- DOUT and DOUT1 are data and clock outputs in normal mode.

If the EM4094 reader chip was in power-down mode before entering normal mode (option bit 1 low or pin EN low) the IC goes through a start-up procedure.
This means that the quartz oscillator is started (or external clock source is enabled), the output driver is enabled and the antenna drivers are checked for short circuit (if bit 5 is set).
After the operation point of the receiver has settled, the DOUT pin goes high for 100µs and then the chip goes to normal mode.
If a short circuit at the antenna driver output is detected, the antenna driver is stopped, DOUT remains low and DOUT1 goes high.

If the EM4094 reader IC was powered-up before SPI communication was started it goes directly to the normal mode.

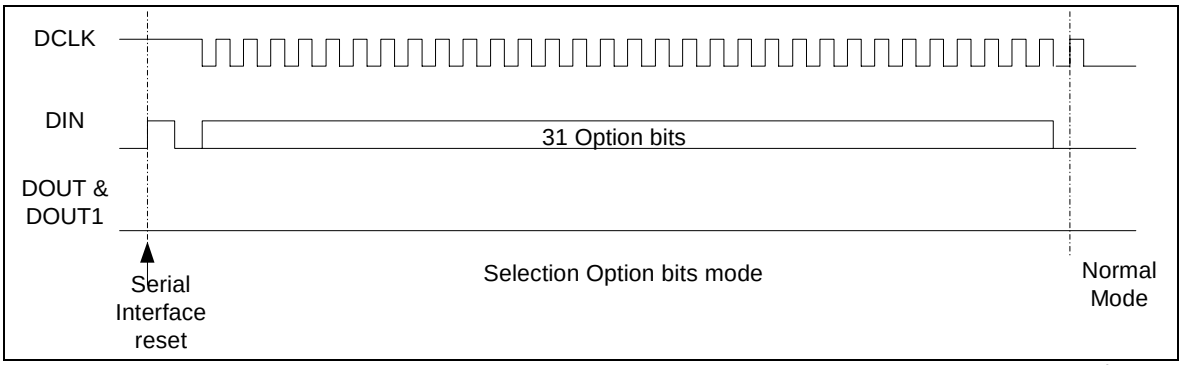


Figure 3

5. Option Bits

The EM4094 system selection bits are:

- Bit 1 Power up flag
- Bit 2 Modulation index selection 0
- Bit 3 Modulation index selection 1
- Bit 4 Modulation index selection 2
- Bit 5 Short circuit protection enable
- Bit 6 Single or dual RF driver selection
- Bit 7 Dual driver in phase or phase phase opposite
- Bit 8 Filter zero selection 1
- Bit 9 Filter zero selection 2
- Bit 10 Filter low pass selection 400kHz
- Bit 11 Receive gain selection 0 (LSB)
- Bit 12 Receiver gain selection 1
- Bit 13 Receiver gain selection 2 (MSB)
- Bit 14 AM / PM input channel selection
- Bit 15 AGC On/Off selection
- Bit 16 AGC attack mode selection
- Bit 17 AGC decay mode selection
- Bit 18 AGC attack rate (lsb)
- Bit 19 AGC attack rate (msb)
- Bit 20 AGC decay wait (lsb)
- Bit 21 AGC decay wait (msb)
- Bit 22 Output selection: direct sub-carrier or BPSK data stream (ISO14443-B)
- Bit 23 BPSK automatic frequency adjust
- Bit 24 Analogue output selection
- Bit 25 Hold delay after modulation selection
- Bit 26 Oscillator gain selection
- Bit 27 External oscillator
- Bit 28 -> 31 Must be set to low level

Power up flag

Bit 1	Description
0	Power down
1	Power up

Output driver configuration
Modulation Index

Bit 4	Bit 3	Bit 2	Description
0	0	0	10% ASK typ.
0	0	1	OOK
0	1	0	ASK decrease 3%
0	1	1	ASK decrease 1.5%
1	0	0	ASK increase 3%
1	0	1	ASK increase 6%
1	1	0	ASK increase 12%
1	1	1	ASK increase 20%

Short Circuit Protection

Bit 5	Description
0	Short circuit protection disabled
1	Short circuit protection enabled

Single or dual RF driver selection

Bit 6	Description
0	ANT1 only
1	ANT1 and ANT2

Dual driver in phase or phase opposite

Bit 7	Description
0	In phase driving
1	Differential driving

Receiving Chain Configuration
Filter zero selection

Bit 9	Bit 8	Description
0	0	High int. zero (~300kHz)
0	1	Mid. int. zero (~200kHz)
1	0	Low int. zero (~100kHz)

Filter low pass selection 400kHz

Bit 10	Description
0	High cut-off frequency (~1 MHz)
1	Mid. cut-off frequency (~400 kHz)

Receive gain selection 0 (Lsb)

Bit 11	Description
0	Nominal gain
1	Gain decreased for 5.7dB

Receive gain selection 1

Bit 12	Description
0	Nominal gain
1	Gain decreased for 11.4dB

Receive gain selection 2 (Msb)

Bit 13	Description
0	Nominal gain
1	Gain decreased for 22.8dB

AM/PM input channel selection

Bit 14	Description
0	RFIN1 input selected
1	RFIN2 input selected

AGC on off selection

Bit 15	Description
0	AGC off
1	AGC on

AGC attack mode selection

Bit 16	Description
0	Attack always
1	First pulse not attacked

AGC decay mode selection

Bit 17	Description
0	Fast decay
1	Slow decay

AGC attack rate

Bit 19	Bit 18	Description
0	0	~19 dB/µs (average)
0	1	~9.5 dB/µs (average)
1	0	~4.7 dB/µs (average)

AGC decay wait

Bit 21	Bit 20	Description
0	0	~44µs
0	1	~88µs
1	0	~176µs

BPSK Decoder
Output selection direct sub-carrier or BPSK 848kHz

Bit 22	Description
0	Sub-carrier
1	BPSK decoder

BPSK automatic frequency adjust

Bit 23	Description
0	Disabled
1	Enabled

Output selection analogue

Bit 24	Description
0	Analogue output disabled
1	Analogue output enabled

Bit 25	Description
0	Hold delay after modulation ~5µs
1	Hold delay after modulation ~15µs

Oscillator
Oscillator gain selection

Bit 26	Description
0	Low gm
1	High gm

External oscillator selection

Bit 27	Description
0	Internal quartz oscillator
1	External oscillator

Note:
It is recommended to set option bits 16 up to bit 21 and option bits 23, 25 to “0”. Bit 26 should be set to “1”.

6. Application information

6.1 Oscillator

The frequency range allowed by the regulations is 13.56MHz ± 7 kHz. The correct load capacitance has to be chosen according to the manufacturer's guideline. COG capacitors should be used. It is not recommended to connect any components except quartz crystal and load capacitors to the oscillator's pins since any interference or noise injected into the oscillator corrupts the system performance.
When an external clock source is used the phase noise of the clock has to be kept low since it also corrupts the system performances.

6.2 Antenna driver

The correct load impedance for a single output driver (100mW) is 7Ω resistive. The correct load impedance for a double parallel output driver (option bit 6, 200mW) is 3.5Ω resistive.
The load impedance for a push-pull driver (bits 6, 7) must be at least 14Ω resistive. In this configuration, the consideration of chip power dissipation and junction temperature is necessary. It is also possible to use this configuration for low power systems with a direct antenna connection if a load impedance higher than 14Ω is used. Since the ASK modulation index is dependent on the load, it will differ from those listed in the table.

6.3 Receiver

Systems using a 212kHz sub-carrier modulation should use the medium filter selection and systems using a 424 kHz or 848kHz sub-carrier should use the high frequency filter selection. When a 424kHz or 848kHz system with on/off sub-carrier coding is used, the higher frequency zero enables very fast response of the receiver to the pulse burst with high DC level shift. When a BPSK system is used, lower frequency zero decreases phase distortion of the BPSK signal.

System option bits control the receiver gain. Different receiver bandwidths result in different noise levels therefore enabling different gain and sensitivity levels. The combination of filter selection and gain selection allows the system designer to choose the best combination for the RFID reader.

6.4. Option bits selection depending transponder IC

The EM4094 transceiver is compliant with almost all 13.56MHz transponder ICs. The large combinations offered by the EM4094 option bits permit to adapt the reader IC to the tag communication protocol.
The below tables give the suggested option bit configuration depending on the transponder IC used.

For an EM4006 read only in double parallel output drive:

Option bit	Suggested value	Configuration
1	1	Power up
2,3,4	1,0,0	OOK modulation
5	1	Short circuit enabled
6,7	1,0	Two drivers in phase
8,9	0,1	100kHz
10	1	400kHz
11,12,13	0,0,0	Nominal gain
14	0	RFIN1 selected
15	1	AGC activated
16 -> 21	0,0,0,0,0,0	Standard configuration
22	0	Sub-carrier mode
23	0	BPSK not used
24	0	Analogue output disable
25	0	Hold delay set to 5us
26	1	High gm
27	0	Internal quartz
28 -> 31	0,0,0,0	Normal IC mode

EM4006 sub-carrier: 26kHz
EM4094 Reception bandwidth: 100kHz – 400kHz
Configuration word value (Hexa): (msb) 02 00 43 33 (lsb)

For ISO15693 standard:

Option bit	Suggested value	Configuration
1	1	Power up
2,3,4	1,0,0	OOK modulation
5	1	Short circuit enabled
6,7	1,0	Two drivers in phase
8,9	0,0	300kHz
10	0	1MHz
11,12,13	0,0,0	Nominal gain
14	0	RFIN1 selected
15	1	AGC activated
16 -> 21	0,0,0,0,0,0	Standard configuration
22	0	Sub-carrier mode
23	0	BPSK not used
24	0	Analogue output disable
25	0	Hold delay set to 5us
26	1	High gm
27	0	Internal quartz
28 -> 31	0,0,0,0	Normal IC mode

Tag sub-carrier: 424kHz or 484kHz
Modulation Index: 100%
Reception bandwidth: 300kHz – 1MHz
AGC: Nominal Gain

Configuration word value (Hexa): (msb) 02 00 40 33 (lsb)
For ISO14443 Type A standard:

Option bit	Suggested value	Configuration
1	1	Power up
2,3,4	1,0,0	OOK modulation
5	1	Short circuit enabled
6,7	1,0	Two drivers in phase
8,9	0,0	300kHz
10	0	1MHz
11,12,13	0,0,0	Nominal gain
14	0	RFIN1 selected
15	1	AGC activated
16 -> 21	0,0,0,0,0,0	Standard configuration
22	0	Sub-carrier mode
23	0	BPSK not used
24	0	Analogue output disable
25	0	Hold delay set to 5us
26	1	High gm
27	0	Internal quartz
28 -> 31	0,0,0,0	Normal IC mode

Tag sub-carrier: 848kHz
Modulation Index: 100%
Reception bandwidth: 300kHz – 1MHz
AGC: Nominal Gain
Configuration word value (Hexa): (msb) 02 00 40 33 (lsb)

For ISO14443 Type C standard:

Option bit	Suggested value	Configuration
1	1	Power up
2,3,4	0,0,1	13% ASK
5	1	Short circuit enabled
6,7	1,0	Two drivers in phase
8,9	0,0	300kHz
10	0	1MHz
11,12,13	0,0,0	Nominal gain
14	0	RFIN1 selected
15	1	AGC activated
16 -> 21	0,0,0,0,0,0	Standard configuration
22	0	Sub-carrier mode
23	0	BPSK not used
24	0	Analogue output disable
25	0	Hold delay set to 5us
26	1	High gm
27	0	Internal quartz
28 -> 31	0,0,0,0	Normal IC mode

Tag sub-carrier: 250kHz
Modulation Index: 13%
Reception bandwidth: 300kHz – 1MHz
AGC: Nominal Gain

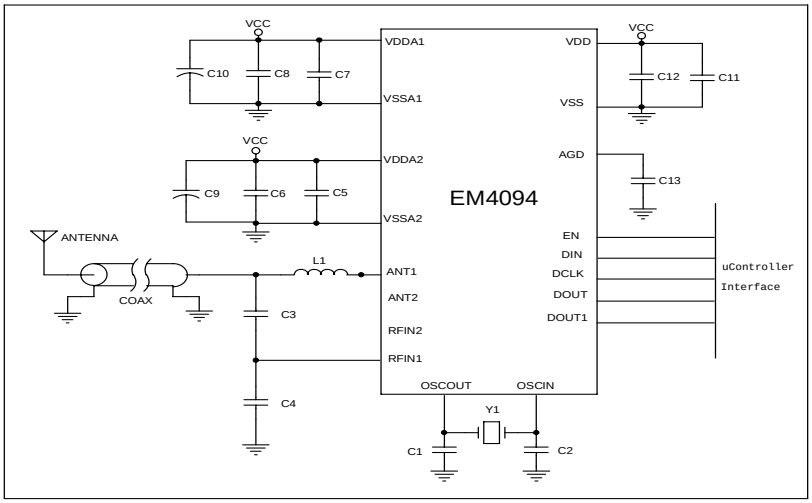
Configuration word value (Hexa): (msb) 02 00 40 3D (lsb)
For ISO14443 Type B standard:

Option bit	Suggested value	Configuration
1	1	Power up
2,3,4	0,0,0	10% ASK
5	1	Short circuit enabled
6,7	1,0	Two drivers in phase
8,9	0,0	300kHz
10	0	1MHz
11,12,13	0,0,0	Nominal gain
14	0	RFIN1 selected
15	1	AGC activated
16 -> 21	0,0,0,0,0,0	Standard configuration
22	0	Sub-carrier mode
23	0	BPSK selected
24	0	Analogue output disable
25	0	Hold delay set to 5us
26	1	High gm
27	0	Internal quartz
28 -> 31	0,0,0,0	Normal IC mode

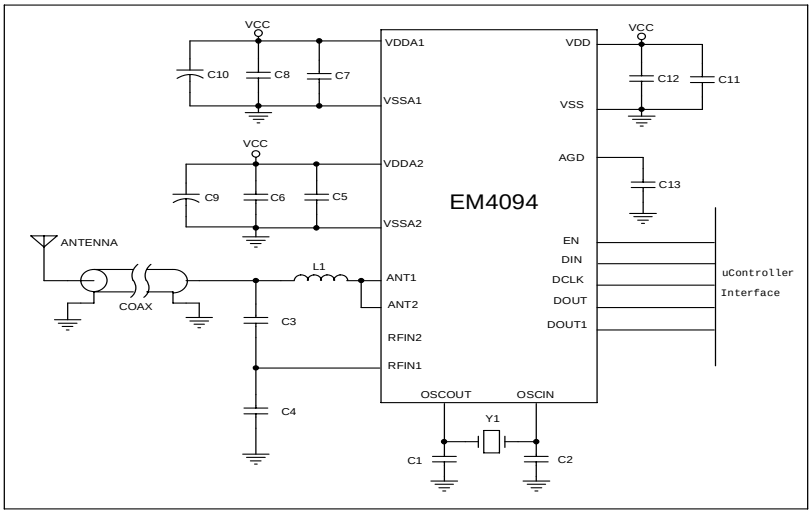
Tag sub-carrier: 848kHz
Modulation Index: 10%
Reception bandwidth: 300kHz – 1MHz
AGC: Nominal Gain
Configuration word value (Hexa): (msb) 02 20 40 31 (lsb)

6.5 Antenna connection configurations

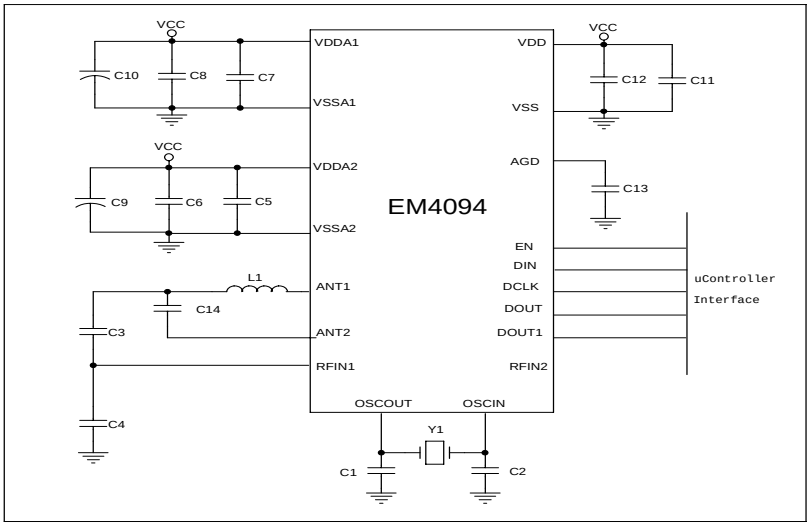
Single Output Driver (100mW)



Double parallel output driver (option bit 6, 200mW)



Configuration for lower power systems with direct antenna connection



In such a configuration, the resonant frequency of the external LC tank has to be tuned accurately to 13.56MHz. The resonant capacitor is composed by C14 in parallel with the capacitor divider (C3 and C4).

7. Pin configuration

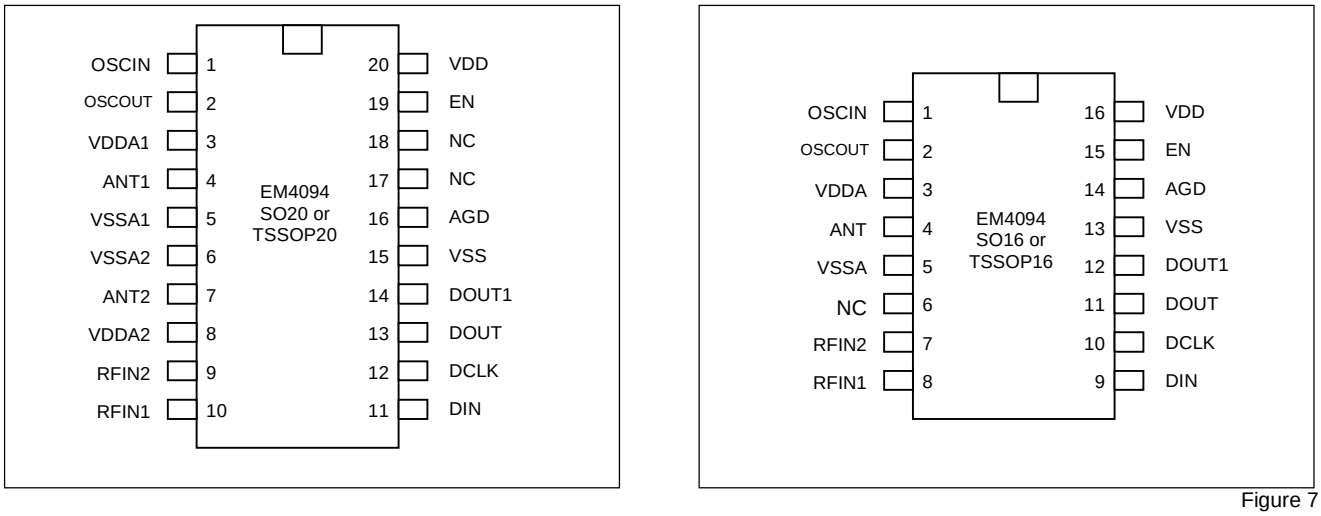


Figure 7

The selection of the package SO16, TSSOP16, TSSOP20 or SO20 depends on the output power level.

8. Pin description

Pin	Name	Description
1	OSCIN	Quartz oscillator input (no internal capacitor)
2	OSCOUT	Quartz oscillator output (no internal capacitor)
3	VDDA1	Positive supply for antenna driver 5V
4	ANT1	RF output (10Ω output impedance)
5	VSSA1	Negative supply for antenna driver 0V
6	VSSA2	Negative supply for antenna driver 0V
7	ANT2	RF output (10Ω output impedance)
8	VDDA2	Positive supply for antenna driver 5V
9	RFIN2	RF input PM (maximum 5Vpp, DC coupled to AGD)
10	RFIN1	RF input AM (maximum 5Vpp, DC coupled to AGD)
11	DIN	SPI Data input / field modulation input
12	DCLK	SPI Data clock
13	DOUT	Digitized receive output / BPSK bit stream output
14	DOUT1	BPSK bit clock output / Analogue receive output
15	VSS	Negative supply 0V
16	AGD	Reference voltage output 2.5V
17	NC	Not used
18	NC	Not used
19	EN	Enable input
20	VDD	Positive supply 5V

Table 5

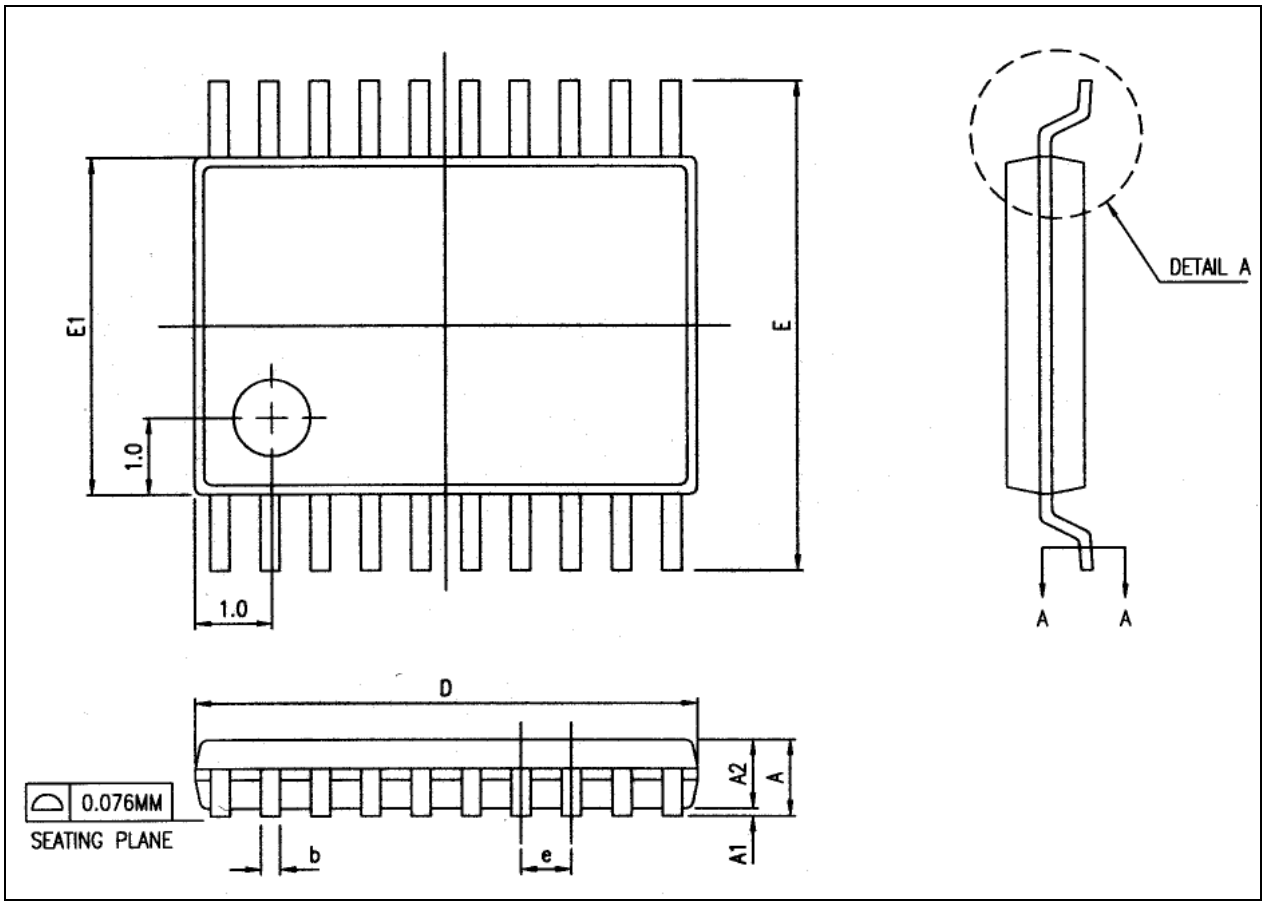
The functionality of pins 13 and 14 is controlled via SPI interface depending on the system demands.

For SO16 and TSSOP16 versions, pins VSSA2, ANT2, VDDA2 are omitted.

All the pins marked NC should be connected to VSS.

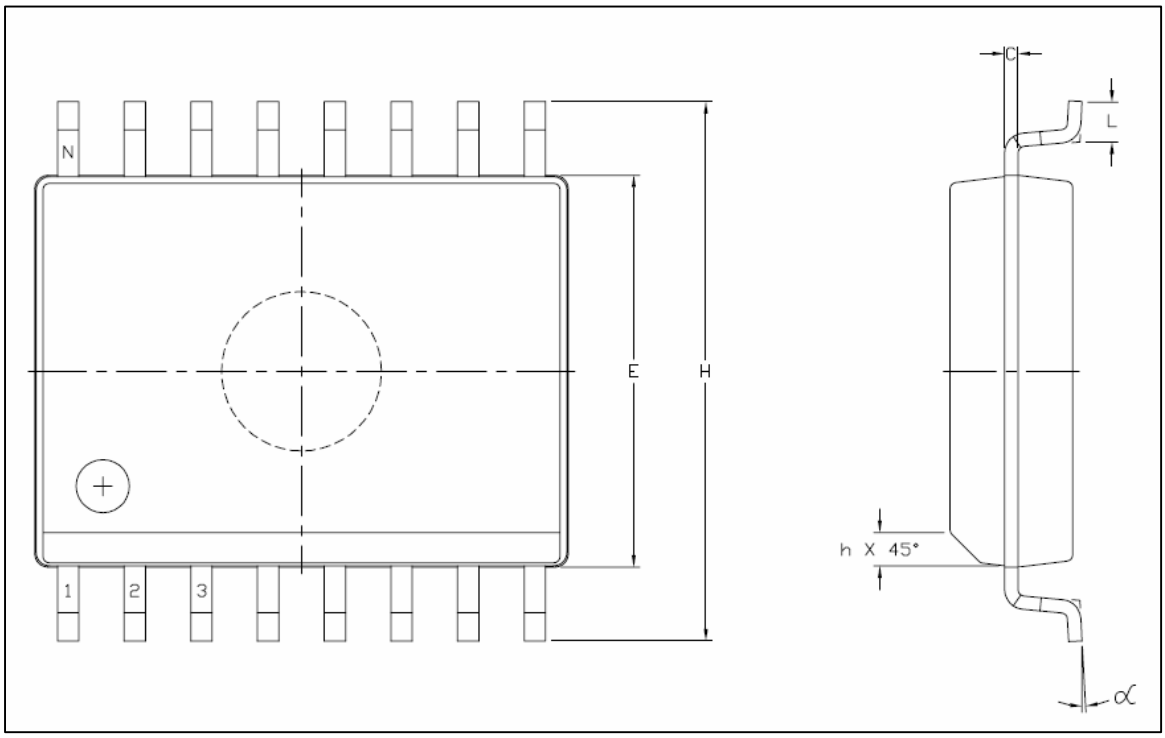
9. Package Information

9.1 TSSO16 – TSSOP20 Package dimensions



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.2			.047
A1	0.05		0.15	.002		.006
A2	0.8	0.9	1.05	.031	.035	.041
b	0.19		0.3	.007		.012
D (TSSOP16)	4.9	5	5.1	.193	.197	.2
D (TSSOP20)	6.4	6.5	6.6	.252	.256	.26
e	0.65 BSC.			.026 BSC.		
E	6.40 BSC.			.252 BSC.		
E1	4.3	4.4	4.5	.169	.173	.177

9.2 SO16 and SO20 Package dimensions



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.35		2.65	.093		.104
A1	0.10		0.30	.004		.012
D (SO16)	10.10		10.50	.398		.413
D (SO20)	12.60		13.00	.496		.512
e	1.27 BSC.			.050 BSC.		
E	7.4		7.6	0.291		.299
H	10.00		10.65	.394		.419

10. Ordering Information

Part Number	Package	Delivery Form
EM4094SO16A	SO16	Stick
EM4094TP16A	TSSOP16	Stick
EM4094SO20A	SO20	Stick
EM4094TP20A	TSSOP20	Stick

11. Product Support

Check our web site under Products/RF Identification section. Questions can be sent to info@emmicroelectronic.com.