Freescale Semiconductor
Data Sheet: Advance Information

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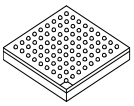
This document contains information on a new product. Specifications and information herein are subject to change without notice. See the latest errata document for details on known device operating limitations.

i.MX 6Dual/6Quad Applications Processors for Consumer Products

Silicon Version 1.0

MCIMX6



Package Information
Plastic Package
Case FCPBGA 21 x 21 mm, 0.8 mm pitch
Case FC PoP 12 x 12 mm, 0.4 mm pitch

Ordering Information
See Table 1 on page 3

1 Introduction

The i.MX 6Dual and i.MX 6Quad processors represent Freescale Semiconductor's latest achievement in integrated multimedia applications processors, which are part of a growing family of multimedia-focused products that offer high performance processing and are optimized for lowest power consumption.

The processors feature Freescale's advanced implementation of the quad ARM™ Cortex-A9 core, which operates at speeds up to 1 GHz. They include 2D and 3D graphics processors, 3D 1080p video processing, and integrated power management. Each processor provides a 64-bit DDR3/LVDDR3-1066 memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, hard drive, displays, and camera sensors.

The i.MX 6Dual/6Quad processors are specifically useful for applications, such as:

- Netbooks (web tablets)
- Nettops (Internet desktop devices)
- High-end mobile Internet devices (MID)

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- High-end PDAs
- High-end portable media players (PMP) with HD video capability
- Gaming consoles
- Portable navigation devices (PND)

The i.MX 6Dual/6Quad processors have some very exciting features, for example:

- Applications processors—The processors enhance the capabilities of high-tier portable applications by fulfilling the ever increasing MIPS needs of operating systems and games. Freescale's Dynamic Voltage and Frequency Scaling (DVFS) provides significant power reduction, allowing the device to run at lower voltage and frequency with sufficient MIPS for tasks, such as audio decode.
- Multilevel memory system—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processors support many types of external memory devices, including DDR3, low voltage DDR3, LPDDR2, NOR Flash, PSRAM, cellular RAM, NAND Flash (MLC and SLC), OneNAND™, and managed NAND, including eMMC up to rev 4.4.
- Smart speed technology—The processors have power management throughout the IC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations.
- Dynamic voltage and frequency scaling—The processors improve the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of each processor is enhanced by a multilevel cache system, Neon MPE (Media Processor Engine) co-processor, a multi-standard hardware video codec, 2 autonomous and independent image processing units (IPU), and a programmable smart DMA (SDMA) controller.
- Powerful graphics acceleration—Each processor provides three independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator with four shaders (up to 200 MT/s and OpenCL support), 2D graphics accelerator, and dedicated OpenVG™ 1.1 accelerator.
- Interface flexibility—Each processor supports connections to a variety of interfaces: LCD controller for up to four displays (including parallel display, HDMI1.4, MIPI display, and LVDS display), dual CMOS sensor interface (parallel or through MIPI), high-speed USB on-the-go with PHY, high-speed USB host PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100/1000 Mbps Gigabit Ethernet controller, and a variety of other popular interfaces (such as UART, I^2C, and I^2S serial audio, SATA-II, and PCIe-II).
- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the i.MX 6Dual/6Quad Security Reference Manual. Contact your local Freescale representative for more information.
- Integrated power management—The processors integrate linear regulators and generate internally all the voltage levels for different domains. This significantly simplifies system power management structure.

1.1 Ordering Information

Table 1 provides ordering information.

Table 1. Ordering Information

Part Number[1]	Mask Set	Features	Package[2]	Market
PCIMX6Q5EVT10AA	N55D	Four core, no codecs or HDCP/DTCP	21 x 21 mm, 0.8 mm pitch BGA Case: Lidded FCPBGA	SMD
PCIMX6D5EVT10AA	N55D	Dual core, no codecs or HDCP/DTCP	21 x 21 mm, 0.8 mm pitch BGA Case: Lidded FCPBGA	SMD
PCIMX6Q5EYM10AA	N55D	Four core, no codecs or HDCP/DTCP	21 x 21 mm, 0.8 mm pitch BGA Case: Non-lidded FCPBGA	SMD
PCIMX6D5EYM10AA	N55D	Dual core, no codecs or HDCP/DTCP	21 x 21 mm, 0.8 mm pitch BGA Case: Non-lidded FCPBGA	SMD
PCIMX6Q5EZK10AA	N55D	Four core, no codecs or HDCP/DTCP	12 x 12 mm, 0.4 mm pitch BGA Case: FC PoP	SMD
PCIMX6D5EZK10AA	N55D	Dual core, no codecs or HDCP/DTCP	12 x 12 mm, 0.4 mm pitch BGA Case: FC PoP	SMD

1 Part numbers with a PC prefix indicate non production engineering parts.

2 Case FCPBGA is RoHS compliant, lead-free MSL (moisture sensitivity level) 3.

1.2 Features

The i.MX 6Dual/6Quad processors are based on ARM Cortex A9 MPCore™ Platform, which has the following features:

- ARM Cortex A9 MPCore™ 4xCPU Processor (with TrustZone)
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor

The ARM Cortex A9 MPCore™ complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 1 MB unified I/D L2 cache, shared by two/four cores
- Two Master AXI (64-bit) bus interfaces output of L2 cache
- Target frequency of the core (including Neon and L1 cache) is:
  - 1 GHz overdrive over the specified temperature range
  - 900 MHz non-overdrive over the specified temperature range
- NEON MPE coprocessor

  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline

The memory system consists of the following components:

- Level 1 Cache—32 KB Instruction, 32 KB Data cache per core
- Level 2 Cache—Unified instruction and data (1 MByte)
- On-Chip Memory:
  - Boot ROM, including HAB (96 KB)
  - Internal multimedia / shared, fast access RAM (OCRAM, 256 KB)
  - Secure/non-secure RAM (16 KB)
- External memory interfaces:
  - 16-bit, 32-bit, and 64-bit DDR3-1066, LV-DDR3-1066, and 1/2 LPDDR2-1066 channels, supporting DDR interleaving mode, for 2x32 LPDDR2-1066
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 32 bit.
  - 16-bit NOR Flash. All WEIMv2 pins are muxed on other interfaces.
  - 16-bit PSRAM, Cellular RAM

Each i.MX 6Dual/6Quad processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Hard Disk Drives—SATA II, 3.0 Gbps
- Displays—Total five interfaces available. Total raw pixel rate of all interfaces is up to 450 Mpixels/sec, 24 bpp. Up to four interfaces may be active in parallel.
  - One Parallel 24-bit display port, up to 225 Mpixels/sec (for example, WUXGA at 60 Hz or dual HD1080 and WXGA at 60 Hz)
  - LVDS serial ports—One port up to 165 Mpixels/sec or two ports up to 85 MP/sec (for example, WUXGA at 60 Hz) each
  - HDMI 1.4 port
  - MIPI/DSI, two lanes at 1 Gbps
- Camera sensors:
  - Parallel Camera port (up to 20 bit and up to 240 MHz peak)
  - MIPI CSI-2 serial camera port, supporting up to 1000 Mbps/lane in 1/2/3-lane mode and up to 800 Mbps/lane in 4-lane mode. The CSI-2 Receiver core can manage one clock lane and up to four data lanes. Each i.MX 6Dual/6Quad processor has four lanes.
- Expansion cards:
  - Four MMC/SD/SDIO card ports all supporting:

  - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
  - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
- USB:
  - High Speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB Phy
  - Three USB 2.0 (480 Mbps) hosts:
    - One HS host with integrated High Speed Phy
    - Two HS hosts with integrated HS-IC USB (High Speed Inter-Chip USB) Phy
- Expansion PCI Express port (PCIe) v2.0 one lane
  - PCI Express (Gen 2.0) dual mode complex, supporting Root complex operations and Endpoint operations. Uses x1 PHY configuration.
- Miscellaneous IPs and interfaces:
  - Three I2S/SSI/AC97, up to 1.4 Mbps each
  - Enhanced Serial Audio Interface (ESAI), up to 1.4 Mbps per channel
  - Five UARTs, up to 4.0 Mbps each:
    - Providing RS232 interface
    - Supporting 9-bit RS485 multidrop mode
    - One of the five UARTs (UART1) supports 8-wire while others four supports 4-wire. This is due to the SoC IOMUX limitation, since all UART IPs are identical.
  - Five eCSPI (Enhanced CSPI), up to 52 Mbps each
  - Three I2C, supporting 400 kbps
  - Gigabit Ethernet Controller (IEEE1588 compliant), 10/100/1000 Mbps
  - Four Pulse Width Modulators (PWM)
  - System JTAG Controller (SJC)
  - GPIO with interrupt capabilities
  - 8x8 Key Pad Port (KPP)
  - Sony Philips Digital Interface (SPDIF), Rx and Tx
  - Two Controller Area Network (FlexCAN), 1 Mbps each
  - Two Watchdog timers (WDOG)
  - Audio MUX (AUDMUX)

The i.MX 6Dual/6Quad processors integrate advanced power management unit and controllers:

- Provide PMU, including DCDC and LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Support DVFS techniques for low power modes
- Use SW State Retention and Power Gating for ARM and MPE
- Support various levels of system power modes
- Use flexible clock gating control scheme

The i.MX 6Dual/6Quad processors use dedicated HW accelerators to meet the targeted multimedia performance. The use of HW accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 6Dual/6Quad processors incorporate the following hardware accelerators:

- VPU—Video Processing Unit
- IPUv3H—Image Processing Unit version 3H (2 IPUs)
- GPU3Dv4—3D Graphics Processing Unit (OpenGL ES 2.0) version 4
- GPU2Dv2—2D Graphics Processing Unit (BitBlt)
- GPUVG—OpenVG 1.1 Graphics Processing Unit
- ASRC—Asynchronous Sample Rate Converter

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- CAAM—Cryptographic Acceleration and Assurance Module, containing 16 KB secure RAM and True and Pseudo Random Number Generator (NIST certified)
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock
- CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSEs and will determine the security level operation mode as well as the TZ policy.
- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

NOTE

The actual feature set depends on the part numbers as described in Table 1, "Ordering Information," on page 3. Functions, such as video hardware acceleration, and 2D and 3D hardware graphics acceleration may not be enabled for specific part numbers.

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6Dual/6Quad processor system.

2.1 Block Diagram

Figure 1 shows the functional modules in the i.MX 6Dual/6Quad processor system.

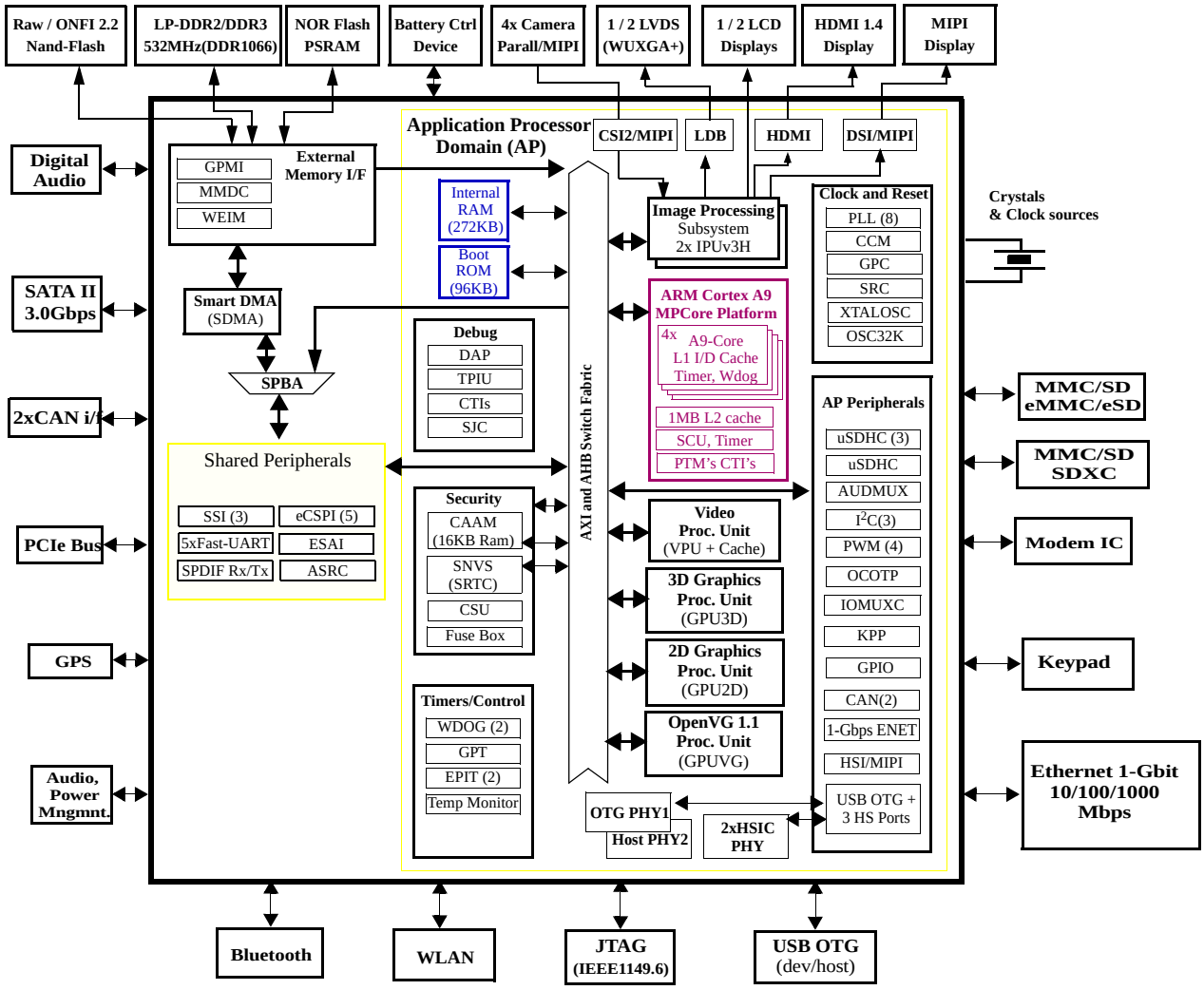


Figure 1. i.MX 6Dual/6Quad System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (2) indicates two separate PWM peripherals.

3 Modules List

The i.MX 6Dual/6Quad processors contain a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX 6Dual/6Quad Modules List

Block Mnemonic	Block Name	Subsystem	Brief Description
ARM	ARM Platform	ARM	The ARM Core Platform consists of 4x (four) Cortex A9 cores and associated sub-blocks, such as the Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, watchdog, and CoreSight debug modules.
APBH-DMA	NAND Flash and BCH ECC DMA controller	System Control Peripherals	DMA controller used for GPMI2 operation
ASRC	Asynchronous Sample Rate Converter	Multimedia Peripherals	The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
BCH40	Binary-BCH ECC Processor	System Control Peripherals	The BCH40 module provides up to 40-bit ECC encryption/decryption for NAND Flash controller (GPMI)
CAAM	Cryptographic accelerator and assurance module	Security	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, and a Pseudo Random Number Generator (PRNG). The pseudo random number generator is certified by Cryptographic Algorithm Validation Program (CAVP) of National Institute of Standards and Technology (NIST). Its DRBG validation number is 94 and its SHS validation number is 1455. CAAM also implements a Secure Memory mechanism. In i.MX 6Dual/6Quad processors, the security memory provided is 16 KB.
CCM GPC SRC	Clock Control Module, Global Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
CSI	MIPI CSI-2 i/f	Multimedia Peripherals	The CSI IP provides MIPI CSI-2 standard camera interface port. The CSI-2 interface supports from 80 Mbps to 800 Mbps speed per data lane.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6Dual/6Quad platform. The Security Control Registers (SCR) of the CSU are set during boot time by the HAB and are locked to prevent further writing.
CTI-0 CTI-1 CTI-2 CTI-3 CTI-4	Cross Trigger Interfaces	Debug / Trace	Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform.
CTM	Cross Trigger Matrix	Debug / Trace	Cross Trigger Matrix IP is used to route triggering events between CTIs. The CTM module is internal to the Cortex-A9 Core Platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform.
DCIC-0 DCIC-1	Display Content Integrity Checker	Automotive IP	The DCIC provides integrity check on portion(s) of the display. Each i.MX 6Dual/6Quad processor has two such modules, one for each IPU.
DSI	MIPI DSI i/f	Multimedia Peripherals	The MIPI DSI IP provides DSI standard display port interface. The DSI interface support 80 Mbps to 1 Gbps speed per data lane.
eCSPI1-5	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
ENET	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 1 Gbit, 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The i.MX 6Dual/6Quad processors also consist of HW assist for IEEE1588 standard. See IEEE1588 section for more details.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
ESAI	Enhanced Serial Audio Interface	Connectivity Peripherals	The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available. The ESAI has 12 pins for data and clocking connection to external devices.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC-1 uSDHC-2 uSDHC-2 uSDHC-4	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX 6Dual/6Quad specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.2/4.3/4.4 including high-capacity (size > 2 GB) cards HC MMC. HW reset as specified for eMMC cards is supported at ports #3 and #4 only. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDHC cards up to 32 GB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v1.10 • Fully compliant with SD Card Specification, Part A2, SD Host Controller Standard Specification, v2.00 All four ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) However, the SoC level integration and I/O muxing logic restrict the functionality to the following: • Instances #1 and #2 are primarily intended to serve as external slots or interfaces to on-board SDIO devices. These ports are equipped with “Card detection” and “Write Protection” pads and do not support HW reset • Instances #3 and #4 are primarily intended to serve interfaces to embedded MMC memory or interfaces to on-board SDIO devices. These ports do not have “Card detection” and “Write Protection” pads and do support HW reset • All ports can work with 1.8 V and 3.3 V cards. There are two completely independent I/O power domains for Ports #1 and #2 in four bit configuration (SD interface). Port #3 is placed in his own independent power domain and port #4 shares power domain with some other interfaces.
FlexCAN-1 FlexCAN-2	Flexible Controller Area Network	Connectivity Peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
512x8 Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables to setup Boot Modes, Security Levels, Security Keys, and many other system parameters. The i.MX 6Dual/6Quad processors consist of 512x8-bit fuse fox accessible through OCOTP_CTRL interface.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6 GPIO-7	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPMI	General Media Interface	Connectivity Peripherals	The GPMI module supports up to 8x NAND devices. 40-bit ECC encryption/decryption for NAND Flash controller (GPMI2). The GPMI supports separate DMA channels per NAND device.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU3Dv4	Graphics Processing Unit, ver.4	Multimedia Peripherals	The GPU3Dv4 provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays up to HD1080 resolution. The GPU3D provides OpenGL ES 2.0, including extensions, OpenGL ES 1.1, and OpenVG 1.1
GPU2Dv2	Graphics Processing Unit-2D, ver 2	Multimedia Peripherals	The GPU2Dv2 provides hardware acceleration for 2D graphics algorithms, such as Bit BLT, stretch BLT, and many other 2D functions.
GPUVGv2	Vector Graphics Processing Unit ver2	Multimedia Peripherals	OpenVG graphics accelerator provides OpenVG 1.1 support as well as other accelerations, including Real-time hardware curve tesselation of lines, quadratic and cubic Bezier curves, 16x Line Anti-aliasing, and various Vector Drawing functions.
HDMI Tx	HDMI Tx i/f	Multimedia Peripherals	The HDMI module provides HDMI standard i/f port to an HDMI 1.4 compliant display.
HSI	MIPI HSI i/f	Connectivity Peripherals	The MIPI HSI provides a standard MIPI interface to the applications processor.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
I^2C-1 I^2C-2 I^2C-3	I^2C Interface	Connectivity Peripherals	I^2C provide serial interface for external devices. Data rates of up to 400 kbps are supported.
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
IPUv3H-1 IPUv3H-2	Image Processing Unit, ver.3H	Multimedia Peripherals	IPUv3H enables connectivity to displays and video sources, relevant processing and synchronization and control capabilities, allowing autonomous operation. The IPUv3H supports concurrent output to two display ports and concurrent input from two camera ports, through the following interfaces: • Parallel Interfaces for both display and camera • Single/dual channel LVDS display interface • HDMI transmitter • MIPI/DSI transmitter • MIPI/CSI-2 receiver The processing includes: • Image conversions: resizing, rotation, inversion, and color space conversion • A high-quality de-interlacing filter • Video/graphics combining • Image enhancement: color adjustment and gamut mapping, gamma correction, and contrast enhancement • Support for display backlight reduction
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8 x 8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
LDB	LVDS Display Bridge	Connectivity Peripherals	LVDS Display Bridge is used to connect the IPU (Image Processing Unit) to External LVDS Display Interface. LDB supports two channels; each channel has following signals: • One clock pair • Four data pairs Each signal pair contains LVDS special differential pad (PadP, PadM).
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Support 16/32/64-bit DDR3-1066 (LV) or LPDDR2-1066 • Supports both dual x32 for LPDDR2 and x64 DDR3 / LPDDR2 configurations (including 2x32 interleaved mode) • Support up to 4 GByte DDR memory space

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
OCOTP_CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.
OCRAM	On-Chip Memory controller	Data Path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module. In i.MX 6Dual/6Quad processors, the OCRAM is used for controlling the 256 KB multimedia RAM through a 64-bit AXI bus.
OSC32KHz	OSC32KHz	Clocking	Generates 32.768 KHz clock from external crystal.
PCIe	PCI Express 2.0	Debug	The PCIe IP provides PCI Express Gen 2.0 functionality.
PMU	Power-Management functions	Data Path	Integrated power management unit. Used to provide power to various SoC domains.
PWM-1 PWM-2 PWM-3 PWM-4	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
RAM 256 KB	Internal RAM	Internal Memory	Internal RAM, which is accessed through OCRAM memory controller.
RAM 16 KB	Secure/non-secure RAM	Secured Internal Memory	Secure/non-secure Internal RAM, interfaced through the CAAM.
ROM 96KB	Boot ROM	Internal Memory	Supports secure and regular Boot Modes. Includes read protection on 4K region for content protection.
ROMCP	ROM Controller with Patch	Data Path	ROM Controller with ROM Patch support
SATA	Serial ATA	Connectivity Peripherals	The SATA controller and PHY is a complete mixed-signal IP solution designed to implement SATA II, 3.0 Gbps HDD connectivity.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast Context-Switching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SJC	System JTAG Controller	System Control Peripherals	The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6Dual/6Quad processors use JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6Dual/6Quad SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SPDIF	Sony Phillips Digital Interface	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface, which is used on the AP to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock / frame sync options. The SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream that reduces CPU overhead in use cases where two time slots are being used simultaneously.
TEMPMON	Temperature Monitor	System Control Peripherals	The temperature monitor/sensor IP, for detecting high temperature conditions
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 4 MHz. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard and the i.MX31 UART modules. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOH3A	USB 2.0 High Speed OTG and 3x HS Hosts	Connectivity Peripherals	USBOH3 contains: • One high-speed OTG module with integrated HS USB PHY • One high-speed Host module with integrated HS USB PHY • Two identical high-speed Host modules connected to HSIC USB ports.
VDOA	VDOA	Multimedia Peripherals	Video Data Order Adapter (VDOA): used to re-order video data from the “tiled” order used by the VPU to the conventional raster-scan order needed by the IPU.
VPU	Video Processing Unit	Multimedia Peripherals	A high-performing video processing unit (VPU), which covers many SD-level and HD-level video decoders and SD-level encoders as a multi-standard video codec engine as well as several important video processing, such as rotation and mirroring. See i.MX61 User Guide for complete list of VPU’s decoding/encoding capabilities.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
WDOG-1	Watch Dog	Timer Peripherals	The Watch Dog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG-2 (TZ)	Watch Dog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode SW.
WEIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The WEIM NOR-FLASH / PSRAM provides: • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
XTALOSC	Crystal Oscillator I/F		The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator to provide USB required frequency.

3.1 Special Signal Considerations

Table 3 lists special signal considerations for the i.MX 6Dual/6Quad processors. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, "Package Information and Contact Assignments." Signal descriptions are defined in the i.MX 6Dual/6Quad reference manual.

Table 3. Special Signal Considerations

Signal Name	Remarks
CLK1_P/CLK1_N; CLK2_P/CLK2_N	Two general purpose differential high speed clock Input/outputs are provided Any or both of them could be used: • To feed external reference clock to the PLLs and further to the modules inside SoC, for example as alternate reference clock for PCIe or/and SATA, Video/Audio interfaces, etc. • To output internal SoC clock to be used outside the SoC as either reference clock or as a functional clock for peripherals, for example it could be used as an output of the PCIe master clock (root complex use) See Anatop and CCM chapters in the i.MX 6Dual/6Quad reference manual for details on the respective clock trees. The clock inputs/outputs are LVDS differential pairs compatible with TIA/EIA-644 standard, the maximal frequency range supported is 0...600MHz. Alternatively one may use single ended signal to drive CLKx_P input. In this case corresponding CLKx_N input should be tied to the constant voltage level equal 1/2 of the input signal swing. Termination should be provided in case of high frequency signals See LVDS pad electrical specification for further details After initialization, the CLKx inputs/outputs could be disabled (if not used) by Anatop register (hw_anadig_ana_misc1). If unused any or both of the CLKx_N/P pairs may be left floating.
RTC_XTALI/RTC_XTALO	If the user wishes to configure CKIL and ECKIL as an RTC oscillator, a 32.768 kHz crystal, (≤50 kΩ ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into RTC_XTALI the RTC_XTALO pin should be left floating or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level and the frequency should be <100 KHz under typical conditions. In case when high accuracy real time clock are not required system may use internal low frequency ring oscillator. It is recommended to connect RTC_XTALI to GND and keep RTC_XTALO floating.
XTALI/XTALO	A 24.0 MHz crystal should be connected between XTALI and XTALO. level and the frequency should be <32 MHz under typical conditions. The crystal must be rated for a maximum drive level of 100 μW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended. Freescale BSP (board support package) software requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTALI must be directly driven by the external oscillator and XTALO is floated. The XTALI signal level must swing from ~0.8 x NVCC_PLL_OUT to ~0.2V. This clock is used as a reference for USB, PCIe, SATA so then there are strict frequency tolerance and jitter requirements. See OSC24M chapter and relevant interface specifications chapters for details

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
DRAM_VREF	When using DDR_VREF with DDR I/O, the nominal reference voltage must be half of the NVCC_DRAM supply. The user must tie DDR_VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_DRAM. Shunt each resistor with a closely-mounted 0.1 µF capacitor. To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the ± 2% DDR_VREF tolerance (per the DDR3 specification) is maintained when four DDR3 ICs plus the i.MX 6Dual/6Quad are drawing current on the resistor divider. It is recommended to use regulated power supply for “big” memory configurations (more that eight devices)
ZQPAD	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND.
NVCC_DRAM_2P5	DDR IO pre-driver 2.5v supply.
VDD_FA FA_ANA	These signals are reserved for Freescale manufacturing use only. User must tie both connections to GND.
JTAG_*nnnn*	The JTAG interface is summarized in Table 2. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.
	JTAG_TDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.
	JTAG_MOD is referenced as SJC_MOD in the i.MX 6Dual/6Quad Reference Manual. Both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. JTAG_MOD set to hi configures the JTAG interface to mode compliant with IEEE1149.1 standard. JTAG_MOD set to low configures the JTAG interface for common SW debug adding all the system TAPs to the chain.
NC	These signals are No Connect (NC) and should be floated by the user.
POR_B	This cold reset negative logic input resets all modules and logic in the IC. May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low)
ON_OFF	In normal mode may be connected to ON/OFF button (De-bouncing provided at this input). Internally this pad is pulled up. Short connection to GND in OFF mode causes internal power management state machine to change state to ON. In ON mode short connection to GND generates interrupt (intended to SW controllable power down). Long above ~5s connection to GND causes “forced” OFF.
TEST_MODE	TEST_MODE is for Freescale factory use. This signal is internally connected to an on-chip pull-down device. The user must either float this signal or tie it to GND.
SATA_REXT	The impedance calibration process requires connection of reference resistor 191 Ω 1% precision resistor on SATA_REXT pad to ground. See additional details in Section “SATA_REXT Reference Resistor Connection” on page 132.
PCIe_REXT	The impedance calibration process requires connection of reference resistor 200 Ω 1% precision resistor on PCIe_REXT pad to ground. See additional details in Section (TBD).

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
CSI_REXT	MIPI CSI PHY reference resistor. Use 6.04 KΩ 1% resistor connected between this pad and GND
DSI_REXT	MIPI DSI PHY reference resistor. Use 6.04 KΩ 1% resistor connected between this pad and GND

Table 4. JTAG Controller Interface Summary

JTAG	I/O Type	On-chip Termination
JTAG_TCK	Input	47 kΩ pull-up
JTAG_TMS	Input	47 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	3-state output	Keeper
JTAG_TRSTB	Input	47 kΩ pull-up
JTAG_MOD	Input	100 kΩ pull-up

3.2 Recommended Connections for Unused Analogue Interfaces

Table 5 shows the recommended connections for any unused analogue interface.

Table 5. Recommended Connections for Unused Analogue Interfaces

Module	Pad Name	Recommendations if Unused?
ANATOP	CLK1_N, CLK1_P, CLK2_N, CLK2_P	Float
CSI	CSI_CLK0M, CSI_CLK0P, CSI_D0M, CSI_D0P, CSI_D1M, CSI_D1P, CSI_D2M, CSI_D2P, CSI_D3M, CSI_D3P, CSI_REXT, CSI_REXTV	Float
DSI	DSI_CLK0M, DSI_CLK0P, DSI_D0M, DSI_D0P, DSI_D1M, DSI_D1P, DSI_REXT, DSI_REXTV	Float
HDMI	HDMI_CLKM, HDMI_CLKP, HDMI_D0M, HDMI_D0P, HDMI_D1M, HDMI_D1P, HDMI_D2M, HDMI_D2P, HDMI_DDCEC, HDMI_HPD, HDMI_REF	Float
	HDMI_VP, HDMI_VPH	Ground
LDB	LVDS0_CLK_N, LVDS0_CLK_P, LVDS0_TX0_N, LVDS0_TX0_P, LVDS0_TX1_N, LVDS0_TX1_P, LVDS0_TX2_N, LVDS0_TX2_P, LVDS0_TX3_N, LVDS0_TX3_P, LVDS1_CLK_N, LVDS1_CLK_P, LVDS1_TX0_N, LVDS1_TX0_P, LVDS1_TX1_N, LVDS1_TX1_P, LVDS1_TX2_N, LVDS1_TX2_P, LVDS1_TX3_N, LVDS1_TX3_P	Float
MLB	MLB_CN, MLB_CP, MLB_DN, MLB_DP, MLB_SN, MLB_SP	Float
PCIe	PCIe_REXT, PCIe_RXM, PCIe_RXP, PCIe_TXM, PCIe_TXP, PCIe_VPTX	Float
	PCIe_VP, PCIe_VPH	Ground

Table 5. Recommended Connections for Unused Analogue Interfaces (continued)

Module	Pad Name	Recommendations if Unused?
RGMII	RGMII_RD0, RGMII_RD1, RGMII_RD2, RGMII_RD3, RGMII_RX_CTL, RGMII_RXC, RGMII_TD0, RGMII_TD1, RGMII_TD2, RGMII_TD3, RGMII_TX_CTL, RGMII_TXC	Float
SATA	SATA_REXT, SATA_RXM, SATA_RXP, SATA_TXM, SATA_TXP	Float
	SATA_VP, SATA_VPH	Ground
USB	USB_H1_DN, USB_H1_DP, USB_H1_VBUS, USB_OTG_CHD_B, USB_OTG_DN, USB_OTG_DP, USB_OTG_VBUS	Float

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6Dual/6Quad processors.

CAUTION

This electrical specification is preliminary. These specifications are not fully tested or guaranteed at this early stage of the product life cycle. Final specifications will be published after thorough characterization and completion of device qualifications.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX 6Dual/6Quad Chip-Level Conditions

For these characteristics, …	Topic appears …
Absolute Maximum Ratings	on page 22
FCPBGA Package Thermal Resistance	on page 22
PoP Package Thermal Resistance	on page 23
Operating Ranges	on page 24
External Clock Sources	on page 26
Maximal Supply Currents	on page 27
Low Power Mode Supply Currents	on page 29
USB PHY Current Consumption	on page 30
SATA Typical Power Consumption	on page 30
PCIe2 Typical Power Consumption	on page 31
HDMI Typical Power Consumption	on page 32

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under Table 7 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the Operating Ranges or Parameters tables is not implied.

Table 7. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Internal supply voltage	VDDARM VDDARM23 VDDSOC	-0.3	1.3	V
Supply voltage GPIO	Supplies denoted as I/O Supply	-0.5	3.6	V
Supply voltage DDR I/O	Supplies denoted as I/O Supply	-0.4	1.975	V
Supply voltage LVDS I/O	Supplies denoted as I/O Supply	-0.3	2.8	V
Supply voltage VDDHIGH_IN	VDDHIGH_IN	-0.3	3.6	V
USB VBUS	VBUS	—	5.25	V
Input voltage on USB_OTG_DP, USB_OTG_DN, USB_H1_DP, USB_H1_DN pins	USB_DP/USB_DN	-0.3	3.63	V
Input/output voltage range	V_{in}/V_{out}	-0.5	OVDD[1]+0.3	V
ESD damage immunity: • Human Body Model (HBM) • Charge Device Model (CDM)	V_{esd}	 — —	 2000 500	V
Storage temperature range	$T_{STORAGE}$	-40	150	°C

1 OVDD is the I/O supply voltage.

4.1.2 Thermal Resistance

4.1.2.1 FCPBGA Package Thermal Resistance

Table 8 provides the FCPBGA package thermal resistance data.

Table 8. FCPBGA Package Thermal Resistance Data

Rating	Board	Symbol	No Lid	Lid	Unit
Junction to Ambient[1] (natural convection)	Single layer board (1s)	$R_{\theta JA}$	31	24	°C/W
	Four layer board (2s2p)	$R_{\theta JA}$	22	15	°C/W
Junction to Ambient[1] (at 200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	24	17	°C/W
	Four layer board (2s2p)	$R_{\theta JMA}$	18	12	°C/W

Table 8. FCPBGA Package Thermal Resistance Data (continued)

Rating	Board	Symbol	No Lid	Lid	Unit
Junction to Board[2]	—	$R_{\theta JB}$	12	5	°C/W
Junction to Case[3] (Top)	—	$R_{\theta JCtop}$	<0.1	1	°C/W

1 Junction-to-Ambient Thermal Resistance was determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-Board Thermal Resistance was determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

3 Junction-to-Case at the top of the package was determined by using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4.1.2.2 PoP Package Thermal Resistance

Table 9 provides the PoP package thermal resistance data.

Table 9. PoP Package Thermal Resistance Data

Rating	Board	Symbol	No Lid	Unit
Junction to Ambient[1] (natural convection)	Single layer board (1s)	$R_{\theta JA}$	41	°C/W
	Four layer board (2s2p)	$R_{\theta JA}$	26	°C/W
Junction to Ambient[1] (at 200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	33	°C/W
	Four layer board (2s2p)	$R_{\theta JMA}$	22	°C/W
Junction to Board[2]	—	$R_{\theta JB}$	13	°C/W
Junction to Case[3] (Top)	—	$R_{\theta JCtop}$	2	°C/W

1 Junction-to-Ambient Thermal Resistance was determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-Board Thermal Resistance was determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

3 Junction-to-Case at the top of the package was determined by using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4.1.3 Operating Ranges

Table 10 provides the operating ranges of the i.MX 6Dual/6Quad processors.

Table 10. Operating Ranges

Parameter Description	Symbol	Min[1]	Typ[2]	Max[3]	Unit	Comment
Input to the ARM Platform and SOC internal regulators. Recommended range for Run mode[4] (VDDARM_IN for cores #0 and #1, VDDARM23_IN for cores #2 and#3).	VDDARM_IN VDDARM23_IN[5] VDDSOC_IN	1.35		1.5	V	LDO Regulator enabled, output set at 1.225V for operation up to 1 GHz.
		1.225		1.3	V	LDO Regulator bypassed for operation up to 1 GHz
Input to the ARM Platform and SOC internal regulators. Recommended range for Standby mode (VDDARM_IN for cores #0 and #1, VDDARM23_IN for cores #2 and#3).	VDDARM_IN VDDARM23_IN[5] VDDSOC_IN	1.0		1.5	V	The Max value denotes the max value which the LDO can withstand, but for power optimization in standby mode a lower value is recommended.
		0.9		1.0	V	LDO Regulator bypassed
Reg1_trg bits field programming value for enabling operation at the max spec'ed frequencies on each domain	Reg1_trg		0x15			(bits 13..9 of the register hw_anadig_reg_core located at ANATOP_BASE_ADDRESS+0 x140)
Input to VDDHIGH internal Regulators	VDDHIGH_IN[6 7 8]	2.7		3.3	V	Must match the range of voltages that the rechargeable backup battery supports.
Input from the backup battery	VDD_SNVS_IN[6 7 8]	2.8		3.3	V	Could be combined with VDDHIGH_IN, if the system does not require keeping real time and other data in OFF state.
VBUS voltage input of USBOTG	USB_OTG_VBUS	4.4		5.25	V	Only required for USB OTG operations.
VBUS voltage input of USB HOST	USB_H1_VBUS	4.4		5.25	V	Only required for USB HOST operations.
DDR I/O supply	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2, DDR3-U
		1.425	1.5	1.575	V	DDR3
		1.283	1.35	1.45	V	DDR3-L
Supply for RGMII I/O power group	NVCC_RGMII	1.14	1.2 or 1.5	1.9		

Table 10. Operating Ranges (continued)

Parameter Description	Symbol	Min[1]	Typ[2]	Max[3]	Unit	Comment
GPIO supplies	NVCC_CSI, NVCC_EIM0, NVCC_EIM1, NVCC_EIM2, NVCC_ENET, NVCC_GPIO, NVCC_LCD, NVCC_NANDF, NVCC_SD1, NVCC_SD2, NVCC_SD3, NVCC_JTAG	1.65	1.8, 2.8, 3.3	3.6	V	
	NVCC_LVDS2P5 NVCC_MIPI	2.25	2.5	2.75	V	
HDMI supplies	HDMI_VP	0.99	1.1	1.21	V	
	HDMI_VPH	2.25	2.5	2.75	V	
PCIe supplies	PCIE_VP	1.023	1.1	1.21	V	
	PCIE_VPH	2.325	2.5	2.75	V	
	PCIE_VPTX	1.023	1.1	1.21	V	
SATA supplies	SATA_VP	0.99	1.1	1.21	V	
	SATA_VPH	2.25	2.5	2.75	V	
Junction temperature	Tj	-20	95[9]	105	°C	

1 The minimum values for the I/O buffer supplies denote their capability, not necessarily the envisioned minimum value in use cases.

2 The typical values for the I/O buffer supplies denote their envisioned typical value in use cases.

3 The maximum values for the I/O buffer supplies denote their capability, not necessarily the envisioned maximum value in use cases for enabling operation at the max spec'ed frequencies on each domain

4 All the parameters denoted as "Run mode" refer to the values required for enabling operation at the max spec'ed frequencies on each domain: ARM Platform 1 GHz, DDR interface at 528 MHz, GPU's-AXI bus, IPU, VPU, VDOA, PCI at 264 MHz, GPU3D shader at 600 MHz, EIM at 133 MHz (under the reservations mentioned in the EIM section of the Electricals AC Timings chapter), RAWNAND at 200 MHz, IPU-MIPI sensor interface at 200 MHz, TPIU at 100 MHz, DCIC at 132 MHz except for parallel port, where timing is met up to 88 MHz, IP bus at 66 MHz, and so on.

5 For Quad core system, connect to VDDARM_IN. For Dual core system, may be shorted to GND together with VDDARM23_CAP to reduce leakage.

6 VDD_SNVS_IN is intended for use with a rechargeable coin cell. If there is no coin cell, VDD_SNVS_IN can be connected to VDDHIGH_IN.

7 When VDDHIGH_IN > VDD_SNVS_IN, a charge current will be applied to the coin cell. An appropriate series device should be added to limit the charging current to acceptable levels. Consult the desired battery specification for more details.

8 If the application uses VDD_SNVS_IN, powered from a regulator, to keep alive the RTC with minimal power consumption, then the design should ensure that VDD_SNVS_IN >= VDDHIGH_IN at all times.

9 Lifetime of 21,900 hours based on 95°C junction temperature, at nominal supply voltages.

Table 11 shows the supplies that can be sourced from the i.MX 6Dual/6Quad on-chip LDO regulators.

Table 11. On-Chip Supplies that can be Sourced from LDO Regulators

Voltage Source	Load	Comment
VDDHIGH_CAP	NVCC_LVDS2P5	Board-level connection to VDDHIGH_CAP
	NVCC_MIPI	
	HDMI_VPH	
	PCIE_VPH	
	SATA_VPH	
VDDSOC_CAP	VDD_CACHE_CAP	Board-level connection to VDDSOC_CAP[1]
	HDMI_VP	
	PCIE_VP	
	PCIE_VPTX	
	SATA_VP	

1 VDDSOC_CAP can only be used to source these supplies as long as it does not exceed 1.21V and VDDARM_CAP/VDDARM23_CAP does not exceed it by more than 50 mV.
If these conditions cannot be met, then an external supply should be used to power these rails.
Recommended use would be to set the VDDSOC LDO to 1.2V and the VDDARM LDO to 1.225V to enable up to 1 GHz operation.
There is no requirement for VDDSOC_CAP to track within 50 mV as long as it is greater than VDDARM_CAP/VDDARM23_CAP.

4.1.4 External Clock Sources

Each i.MX 6Dual/6Quad processor has two external input system clocks: a low frequency (CKIL) and a high frequency (XTAL).

The CKIL is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can substitute the CKIL, in case accuracy is not important.

The system clock input XTAL is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

Table 12 shows the interface frequency requirements.

Table 12. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
CKIL Oscillator[1]	f_{ckil}	—	32.768[2]/32.0	—	kHz
XTAL Oscillator[3]	f_{xtal}		24		MHz

1 External oscillator or a crystal with internal oscillator amplifier.

2 Recommended nominal frequency 32.768 kHz.

3 External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 12 are required for use with Freescale BSPs to ensure precise time keeping and USB operation. For CKIL operation, two clock sources are available:

- On-chip 40 kHz ring oscillator: This clock source has the following characteristics:
  - Approximately 25 µA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit
  - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator
  - If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision timeout.

4.1.5 Maximal Supply Currents

Table 13 shows the maximal momentary current transients on power lines, and should be used for power supply selection. The Power Virus numbers in Table 13 represent a use case with very high power consumption, which is far higher than the average power consumption in typical use cases. Although the Power Virus numbers shown are theoretically possible, the Drhystone numbers are more likely to represent a typical use case. See i.MX 6Dual/6Quad power consumption application note for more details on typical power consumption.

Table 13. Maximal Supply Currents

Power Line	Conditions	Max Current	Unit
VDDARM_IN+VDDARM23_IN	1 GHz ARM clock based on Power Virus operation	3920	mA
	1 GHz ARM clock based on Drhystone operation	2270	mA
VDDSOC_IN	1 GHz ARM clock	1890	mA
VDDHIGH_IN	—	30[1]	mA
VDD_SNVS_INS	—	1[2]	mA
USB_OTG_VBUS/USB_H1_VBUS (LDO 3P0)	—	25[3]	mA
Primary Interface (IO) Supplies			
NVCC_DRAM		TBD	
NVCC_ENET	N=10	Use maximal IO Equation[4]	
NVCC_LCD	N=29	Use maximal IO Equation[4]	
NVCC_GPIO	N=24	Use maximal IO Equation[4]	

Table 13. Maximal Supply Currents (continued)

NVCC_CSI	N=20	Use maximal IO Equation[4]	
NVCC_EIM0	N=19	Use maximal IO Equation[4]	
NVCC_EIM1	N=14	Use maximal IO Equation[4]	
NVCC_EIM2	N=20	Use maximal IO Equation[4]	
NVCC_JTAG	N=6	Use maximal IO Equation[4]	
NVCC_RGMII	N=12	Use maximal IO Equation[4]	
NVCC_SD1	N=6	Use maximal IO Equation[4]	
NVCC_SD2	N=6	Use maximal IO Equation[4]	
NVCC_SD3	N=11	Use maximal IO Equation[4]	
NVCC_NANDF	N=26	Use maximal IO Equation[4]	
NVCC_MIPI		TBD	
MISC			
DDR_VREF		TBD	

1 The actual maximum current drawn from VDDHIGH_IN will be as shown plus any additional current drawn from the VDDHIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_LVDS2P5, NVCC_MIPI, or HDMI, PCIe, and SATA VPH supplies).

2 This is the maximum current in normal run mode and not the current drawn in low power mode or expected to be supplied by a coin cell.

3 This is the maximum current per active USB physical interface.

4 General Equation for estimated, maximal power consumption of an IO power supply:
Imax = N x C x V x (0.5 x F)
Where:
N—Number of IO pins supplied by the power line
C—Equivalent external capacitive load
V—IO voltage
(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F).

4.1.6 Low Power Mode Supply Currents

Table 14 shows the current core consumption (not including I/O) of i.MX 6Dual/6Quad processors in selected low power modes.

Table 14. Stop Mode Current and Power Consumption[1]

Mode	Conditions	VDDARM_IN		VDDSOC_IN		PLL		Unit
		Typ[2]	Max[3]	Typ[2]	Max[3]	Typ[2]	Max[3]	
WAIT	• Clocks are gated. • DDR is in self refresh. • Three system PLLs are active in bypass (24 MHz). • Supply Voltages remain ON.							mA
STOP	• PLLs disabled • CPU voltage is down to 0.9 V using internal regulator • DDR is in self refresh							mA
Standby	• PLLs disabled • Low voltage • Well Bias ON • CPU regulator disabled for power gating • GPUs and VPU regulator disabled in S/W • SoC regulator bypass • XTAL enabled							mA
Deep Sleep Mode	• PLLs disabled • Low voltage • Well Bias ON • CPU regulator disabled for power gating • GPUs and VPU regulator disabled in S/W • SoC regulator bypass • XTAL disabled • Bandgap disabled							mA
SRTC mode	• SoC is powered down. Only SNVS domain is powered.							mA

1 The data in this table will be finalized after the complete characterization of the silicon.

2 Typical column: T_A = 25°C

3 Maximum column: T_A = 85°C

4.1.7 USB PHY Current Consumption

4.1.7.1 Power Down Mode

In power down mode, everything is powered down, including the VBUS valid detectors, typ condition. Table 15 shows the USB interface current consumption in power down mode.

Table 15. USB PHY Current Consumption in Power Down Mode

	VDDUSB_CAP (3.0 V)	VDDHIGH_CAP (2.5 V)	NVCC_PLL_OUT (1.1 V)
Current	5.1 µA	1.7 µA	<0.5 µA

NOTE

The currents on the VDDHIGH_CAP and VDDUSB_CAP were identified to be the voltage divider circuits in the USB-specific level shifters.

4.1.8 SATA Typical Power Consumption

Table 16 provides typical power consumption values for the SATA PHY when operating at 33 ºC in various Tx modes of operation at the typical-typical process corner.

NOTE

Tx power consumption values are provided for a single transceiver. If T = single transceiver power and C = Clock module power, the total power required for N lanes = N x T + C.

Table 16. SATA Typical Power Consumption with 2.5 V I/O's

Tx Power Mode	Transceiver			Clock Module			Unit
	Total	SATA_VP	SATA_VPH	Total	SATA_VP	SATA_VPH	
P0: Full-power state[1]	44.309	12.31	31.999	23.142	7.572	15.57	mW
P0: Mobile[2]	39.743	12.31	27.433	23.142	7.572	15.57	mW
P0s: Transmitter idle	17.626	10.334	7.292	23.142	7.572	15.57	mW
P1: Transmitter idle, Rx powered down, LOS disabled	1.324	0.739	0.585	23.142	7.572	15.57	mW
P2: Powered-down state, only LOS and POR enabled	0.864	0.584	0.28	0.333	0.04	0.293	mW
PDDQ mode[3]	0.043	0.0141	0.0288	0.019	0.009	0.010	mW

1 Programmed for 1.0 V peak-to-peak Tx level.

2 Programmed for 0.9 V peak-to-peak Tx level with no boost or attenuation.

3 LOW power non-functional.

4.1.9 PCIe2 Typical Power Consumption

Table 17 provides estimated power consumption values for a PCIe2 PHY one-port macro that uses the 1.1 V and 2.5 V power supply option, implemented in the TSMC 40LP 1.1/2.5-V process. The typical values have been obtained through simulation at room temperature, using the typical process corner, nominal analog, and digital power supply levels, and a PCIe channel attached to the PHY. The worst case values have been obtained through simulation from -40°C to 125°C, across process corners, and power supply levels.

Table 17. PCIe2 PHY Power Consumption

MODE		Current from VP 1.1V (in mA)	Current from VPTX 1.1V (in mA)	Current from VPH 2.5V (in mA)	Total Current (in mA)	Total Power Consumption (in mE)
P0: Normal Operation	5G Typ	26.3	14.8	13.1	54.2	78.0
	5G W.C.	39.9	19.9	21.4	81.3	119.2
	2.5G Typ	18.3	14.8	12	45.1	66.4
	2.5G W.C.	27.3	19.9	20.0	67.2	101.9
P0s: Low Recovery Time Latency, Power Saving State	5G Typ	18.3	1.49	10.7	30.5	48.5
	5G W.C.	29.5	2.44	18.4	50.4	81.2
	2.5G Typ	12.7	1.49	10.7	24.9	42.3
	2.5G W.C.	20.0	2.44	18.4	40.7	70.6
P1: Longer Recovery Time Latency, Lower Power State	Typical	7.6	1.49	6.1	15.2	25.3
	W.C.	11.5	2.44	12.4	26.4	46.4
P2: Lowest Power State	Typical	1.65	0.00	0.32	2.0	2.6
	W.C.	2.74	0.17	1.23	4.1	6.3
Power Down	Typical	0.030	0.003	0.001	0.034	0.038
	W.C.	1.271	0.175	0.364	1.810	2.501

4.1.10 HDMI Typical Power Consumption

Table 18 provides power consumption values for the HDMI 3D Tx PHY. Measurements were taken with the HDMI 3D Tx PHY, transmitting an LFSR15 data pattern.

Table 18. HDMI PHY Power Consumption

Mode			Typical	Maximum	Unit
Active mode	Bit rate at 251.75 Mbps	ICC (VPH)	12.7	13.7	mA
		ICC (VP)	2.8	4.1	mA
	Bit rate at 270.27 Mbps	ICC (VPH)	13	14	mA
		ICC (VP)	2.92	4.23	mA
	Bit rate at 742.5 Mbps	ICC (VPH)	15.3	16.5	mA
		ICC (VP)	5.77	7.45	mA
	Bit rate at 1.485 Gbps	ICC (VPH)	15.4	16.6	mA
		ICC (VP)	10.1	12.3	mA
	Bit rate at 2.275 Gbps	ICC (VPH)	15	16.3	mA
		ICC (VP)	14.6	17.4	mA
	Bit rate at 2.97 Gbps	ICC (VPH)	17	18.5	mA
		ICC (VP)	18.9	22.2	mA
Power-down mode	ICC (VPH)		13.7	49.3	μA
	ICC (VP)		55.7	1116	μA

4.2 Power Supplies Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

4.2.1 Power-Up Sequence

For power-up sequence, the restrictions are as follows:

- VDD_SNVS_IN supply must be turned ON before any other power supply. It may be connected (shorted) with VDDHIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- If VDDARM_IN and VDDSOC_IN are connected to different external supply sources, then the following restrictions apply:
  - VDDARM_IN supply must be turned ON together with VDDSOC_IN supply or not delayed more than 1 ms
  - VDDARM_CAP must not exceed VDDSOC_CAP by more than 50 mV.

NOTE

The POR_B input (if used) must be immediately asserted at power-up and remain asserted until the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control. See the i.MX 6Dual/6Quad reference manual for further details and to ensure that all necessary requirements are being met.

NOTE

Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

4.2.2 Power-Down Sequence

No special restrictions for i.MX 6Dual/6Quad IC.

4.2.3 Power Supplies Usage

- All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Group” column of Table 96, "21 x 21 mm Functional Contact Assignments," on page 159.
- When SATA interface and embedded thermal sensor are not used, the SATA_VP and SATA_VPH supplies should be grounded. The input and output supplies for rest of the ports (SATA_REFCLKM, SATA_REFCLKP, SATA_REXT, SATA_RXM, SATA_RXP, and SATA_TXM) can be left floating. It is recommended not to turn OFF the SATA_VPH supply while the SATA_VP supply is ON, as it may lead to excessive power consumption.

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. See the i.MX 6Dual/6Quad reference manual for details on the power tree scheme.

4.3.1 Digital Regulators (LDO_ARM, LDO_PU, LDO_SOC)

There are three digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of their input supply ripple rejection and their on die trimming. This translates into more voltage for the die producing higher operating frequencies. These regulators have three basic modes.

- Bypass. The regulation FET is switched fully on passing the external voltage, DCDC_LOW, to the load unaltered. The analog part of the regulator is powered down in this state, removing any loss other than the IR drop through the power grid and FET.
- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.

- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the programmed target voltage. The target voltage is fully programmable in 25 mV steps.

For additional information, see the reference manual.

4.3.2 Analog Regulators

4.3.2.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from a higher analog supply voltage (2.8 V–3.3 V) to produce a nominal 1.1 V output voltage. The output of the regulator can be programmed in 25 mV steps from 0.8 V to 1.4 V and can provide up to 150 mA output current with a 300 mV drop-out voltage. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 µF (2.2 µF should be considered the recommended minimum value), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For additional information, see the reference manual.

4.3.2.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from a higher analog supply voltage (2.8 V–3.3 V) to produce a nominal 2.5 V output voltage. The output of the regulator can be programmed in 25 mV steps from 2.0 V to 2.75 V and can provide up to 350 mA output current with a 500 mV drop-out voltage. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 µF (2.2 µF should be considered the recommended minimum value), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω.

For additional information, see the reference manual.

4.3.2.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB VBUS voltages (4.5 V–5 V) to produce a nominal 3.0 V output voltage. The output of the regulator can be

programmed in 25 mV steps from 2.625 V to 3.4 V and can provide up to 50 mA output current with a 500 mV drop-out voltage. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 µF (2.2 µF should be considered the recommended minimum value), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either VBUS supply, when both are present. If only one of the VBUS voltages is present, then, the regulator automatically selects this supply. Current limit is also included to help the system meet in-rush current targets.

For additional information, see the reference manual.

4.4 PLL's Electrical Characteristics

4.4.1 Audio/Video PLL's Electrical Parameters

Table 19. Audio/Video PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.2 528 MHz PLL

Table 20. 528 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.3 Ethernet PLL

Table 21. Ethernet PLL's Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.4 480 MHz PLL

Table 22. 480 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<383 reference cycles

4.4.5 ARM PLL

Table 23. ARM PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz~1.3 GHz
Reference clock	24 MHz
Lock time	<2250 reference cycles

4.5 On-Chip Oscillators

4.5.1 OSC24M

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a oscillator. The oscillator is powered from NVCC_PLL_OUT.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

4.5.2 OSC32K

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery (VDD_SNVS_IN) or VDDHIGH_IN such as the oscillator consumes power from VDDHIGH_IN when that supply is available and transitions to the back up battery when VDDHIGH_IN is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 K will automatically switch to a crude internal ring oscillator. The frequency range of this block is approximately 10–45 KHz. It highly depends on the process, voltage, and temperature.

The OSC32k runs from VDD_SNVS_CAP, which comes from the VDDHIGH_IN/VDD_SNVS_IN power mux. The target battery is a ~3 V coin cell. Proper choice of coin cell type is necessary for chosen VDDHIGH_IN range. Appropriate series resistor (Rs) must be used when connecting the coin cell. Rs

depends on the charge current limit that depends on the chosen coin cell. For example, for Panasonic ML621:

- Average Discharge Voltage is 2.5 V
- Maximum Charge Current is 0.6 mA

For a charge voltage of 3.2 V, Rs = (3.2-2.5)/0.6 m = 1.17 k

NOTE

Always refer to the chosen coin cell manufacturer's data sheet for the latest information.

Table 24. OSC32K Main Characteristics

	Min	Typ	Max	Comments
Fosc		32.768 KHz		This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well.
Current consumption		45 μA		The typical value shown is for the oscillator driven by an external crystal. If the internal ring oscillator is used instead of an external crystal, then approximately 25 μA should be added to this value.
Bias resistor		14 MΩ		This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Crystal Properties				
Cload		10 pF		Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR		50 kΩ		Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3 modes
- LVDS I/O

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output.

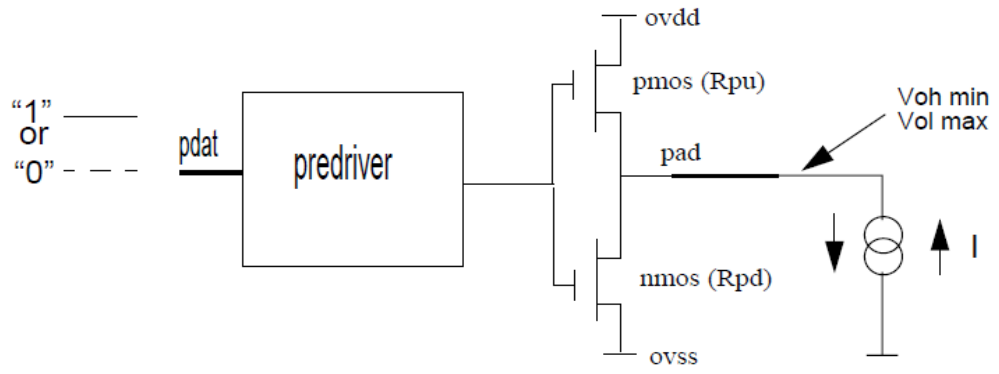


Figure 2. Circuit for Parameters Voh and Vol for I/O Cells

4.6.1 General Purpose I/O (GPIO) DC Parameters

The parameters in Table 25 are guaranteed per the operating ranges in Table 7, unless otherwise noted. Table 25 shows DC parameters for GPIO pads, operating at supply range 1.1 V to 3.6 V (1.2/1.8/3.3 V nom).

Table 25. GPIO I/O DC Parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High-level output voltage[1]	Voh	Iout = –1 mA	OVDD – 0.15	—	—	V
Low-level output voltage[1]	Vol	Iout = 1 mA	—	—	0.15	V
High-Level DC input voltage[1, 2]	Vih	—	0.7 × OVDD	—	OVDD	V
Low-Level DC input voltage[1, 2]	Vil	—	0	—	0.3 × OVDD	V
Input Hysteresis	Vhys	OVDD = 1.8 V OVDD = 3.3 V	0.25	—	—	V
Schmitt trigger VT+[2, 3]	VT+	—	0.5 × OVDD	—	—	V
Schmitt trigger VT–[2, 3]	VT–	—	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	Iin	Vin = OVDD or 0	—	0.05	38	nA
Input current (22 kΩ Pull-up)	Iin	Vin = 0 V Vin = OVDD	—	77 0.05	212 1	μA
Input current (47 kΩ Pull-up)	Iin	Vin = 0 V Vin = OVDD	—	36 0.05	100 1	μA
Input current (100 kΩ Pull-up)	Iin	Vin = 0 V Vin= OVDD	—	18 0.05	48 1	μA
Input current (100 kΩ Pull-down)	Iin	Vin = 0 V Vin = OVDD	—	0.05 17	1 48	μA
Keeper Circuit Resistance			105	130[4]	165	kΩ

1 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

2 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

3 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4 Use an off-chip pull resistor of 10 kΩ or less to override this keeper.

4.6.2 DDR I/O DC Parameters

The DDR I/O pads support LPDDR2 and DDR3 operational modes.

4.6.2.1 LPDDR2 Mode I/O DC Parameters

The LPDDR2 interface mode fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009.

Table 26. LPDDR2 I/O DC Electrical Parameters[1]

Parameters	Symbol	Test Conditions	Min	Typ	Max	Unit
High-level output voltage	Voh	—	0.9*OVDD	—	—	V
Low-level output voltage	Vol	—	—	—	0.1*OVDD	V
Input Reference Voltage	Vref		0.49*OVDD	0.5*OVDD	0.51*OVDD	
DC input High Voltage	Vih(dc)	—	Vref+0.13V	—	OVDD	V
DC input Low Voltage	Vil(dc)	—	OVSS	—	Vref-0.13V	V
Differential Input Logic High	Vih(diff)		0.26		See Note [2]	
Differential Input Logic Low	Vil(diff)		See Note [2]		-0.26	
Input current (no pull-up/down)	Iin	Vin = 0 or OVDD	—	3.5	2000	nA
Pull-up/Pull-down impedance Mismatch	MMpupd		-15		+15	%
240 Ω unit calibration resolution	Rres				10	Ω
Keeper Circuit Resistance	Rkeep	—	110	140[3]	170	kΩ

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

3 Use an off-chip pull resistor of 10 kΩ or less to override this keeper.

4.6.2.2 DDR3 Mode I/O DC Parameters

The DDR3 interface mode fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008. The parameters in Table 27 are guaranteed per the operating ranges in Table 7, unless otherwise noted.

Table 27. DDR3 I/O DC Electrical Parameters

Parameters	Symbol	Test Conditions	Min	Typ	Max	Unit
High-level output voltage	Voh	—	0.8*OVDD[1]	—	—	V
Low-level output voltage	Vol	—	—	—	0.2*OVDD	V
DC input Logic High	Vih(dc)	—	Vref[2]+0.1	—	OVDD	V
DC input Logic Low	Vil(dc)	—	OVSS	—	Vref-0.1	V
Differential input Logic High	Vih(diff)	—	0.2	—	See Note[3]	V
Differential input Logic Low	Vil(diff)	—	See Note[3]	—	-0.2	V
Termination Voltage	Vtt	Vtt tracking OVDD/2	0.49*OVDD	Vref	0.51*OVDD	V
Input current (no pull-up/down)	Iin	Vin = 0 or OVDD	—	4	2900	nA
Pull-up/Pull-down impedance mismatch	MMpupd	—	-10	—	10	%
240 Ω unit calibration resolution	Rres	—	—	—	10	Ω
Keeper Circuit Resistance	Rkeep	—	105	130[4]	165	kΩ

1 OVDD – I/O power supply (1.425 V–1.575 V for DDR3)

2 Vref – DDR3 external reference voltage

3 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

4 Use an off-chip pull resistor of 10 kΩ or less to override this keeper.

4.6.3 LVDS I/O DC Parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

Table 28 shows the Low Voltage Differential Signaling (LVDS) I/O DC parameters.

Table 28. LVDS I/O DC Parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Differential Voltage	V_{OD}	Rload=100 Ω between padP and padN	250	350	450	mV
Output High Voltage	V_{OH}		1.25	1.375	1.6	V
Output Low Voltage	V_{OL}		0.9	1.025	1.25	
Offset Voltage	V_{OS}		1.125	1.2	1.375	

4.7 I/O AC Parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3 modes
- LVDS I/O

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 3 and Figure 4.

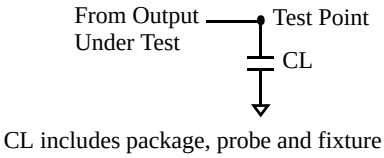


Figure 3. Load Circuit for Output

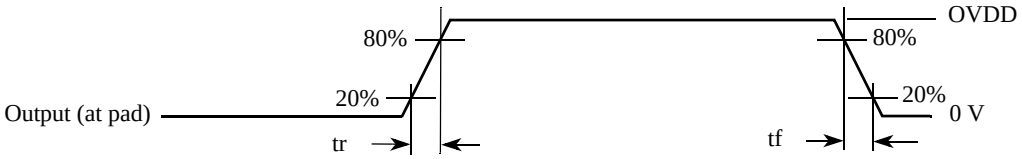


Figure 4. Output Transition Time Waveform

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 29 and Table 30, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 29. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times[1]	trm	—	—	—	25	ns

[1] Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 30. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	
Input Transition Times[1]	trm	—	—	—	25	ns

[1] Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.7.2 DDR I/O AC Parameters

The LPDDR2 interface mode fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3 interface mode fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 31 shows the AC parameters for DDR I/O operating in LPDDR2 mode.

Table 31. DDR I/O LPDDR2 Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref – 0.22	V
AC differential input high voltage[2]	Vidh(ac)	—	0.44	—	—	V
AC differential input low voltage	Vidl(ac)	—	—	—	0.44	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	-0.12	—	0.12	V
Over/undershoot peak	Vpeak	—	—	—	0.35	V
Over/undershoot area (above OVDD or below OVSS)	Varea	533 MHz	—	—	0.3	V-ns
Single output slew rate, measured between Vol(ac) and Voh(ac)	tsr	50 Ω to Vref. 5pF load. Drive impedance = 40 Ω +-30%	1.5	—	3.5	V/ns
		50 Ω to Vref. 5pF load.Drive impedance = 60 Ω +-30%	1	—	2.5	
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk=533MHz	—	—	0.1	ns

[1] Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage |Vtr – Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) – Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 * OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 32 shows the AC parameters for DDR I/O operating in DDR3 mode.

Table 32. DDR I/O DDR3 Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.175	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref – 0.175	V
AC differential input voltage[2]	Vid(ac)	—	0.35	—	—	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	Vref – 0.15	—	Vref + 0.15	V
Over/undershoot peak	Vpeak	—	—	—	0.4	V
Over/undershoot area (above OVDD or below OVSS)	Varea	533 MHz	—	—	0.5	V-ns
Single output slew rate, measured between Vol(ac) and Voh(ac)	tsr	Driver impedance = 34 Ω	2.5	—	5	V/ns
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk=533MHz	—	—	0.1	ns

1 Note that the JEDEC JESD79_3C specification supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) – Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 * OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4.7.3 LVDS I/O AC Parameters

The differential output transition time waveform is shown in Figure 5.

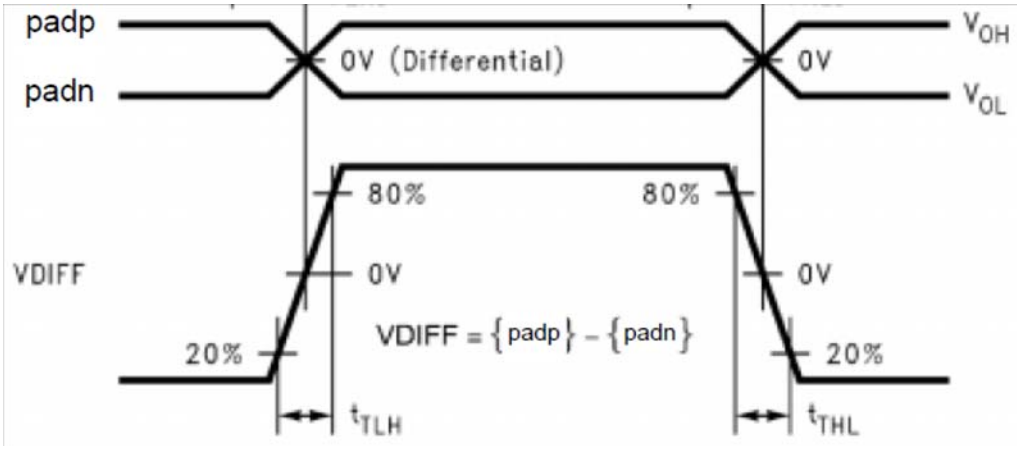


Figure 5. Differential LVDS Driver Transition Time Waveform

Table 33 shows the AC parameters for LVDS I/O.

Table 33. I/O AC Parameters of LVDS Pad

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential pulse skew[1]	t_{SKD}	Rload = 100 Ω, Cload = 2 pF	—	—	0.25	ns
Transition Low to High Time[2]	t_{TLH}		—	—	0.5	
Transition High to Low Time[2]	t_{THL}		—	—	0.5	
Operating Frequency	f	—	—	600	800	MHz
Offset voltage imbalance	Vos	—	—	—	150	mV

1 t_{SKD} = | t_{PHLD} – t_{PLHD} |, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

2 Measurement levels are 20-80% from output voltage.

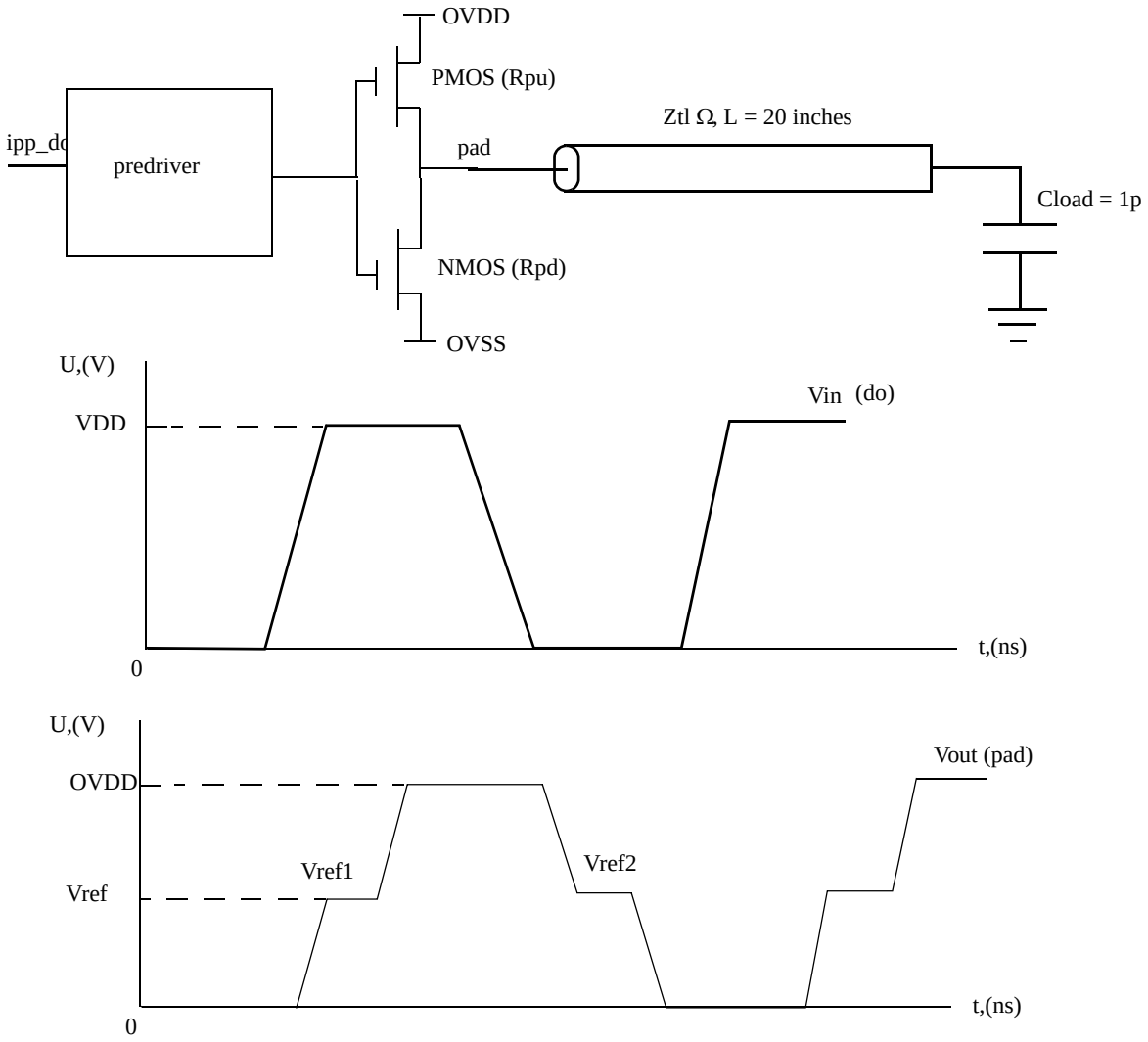
4.8 Output Buffer Impedance Parameters

This section defines the I/O impedance parameters of the i.MX 6Dual/6Quad processors for the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2, and DDR3 modes
- LVDS I/O

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 6).



$$Rpu = \frac{Vovdd - Vref1}{Vref1} \times Ztl$$

$$Rpd = \frac{Vref2}{Vovdd - Vref2} \times Ztl$$

Figure 6. Impedance Matching Load for Measurement

4.8.1 GPIO Output Buffer Impedance

Table 34 shows the GPIO output buffer impedance (OVDD 1.2 V).

Table 34. GPIO Output Buffer Average Impedance (OVDD 1.2 V)

Parameter	Symbol	Drive Strength (ipp_dse)	Min	Typ	Max	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	315 160 105 75 60 50 43	500 250 165 125 100 82 70	800 400 270 190 150 130 110	Ω

Table 35 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 35. GPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (ipp_dse)	Min	Typ	Max	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	160 80 53 42 33 28 24	260 130 90 60 50 40 33	400 200 132 104 83 70 55	Ω

Table 36 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 36. GPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (ipp_dse)	Min	Typ	Max	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	116 58 39 30 24 20 17	150 75 50 37 30 25 20	220 110 73 58 46 38 32	Ω

4.8.2 DDR I/O Output Buffer Impedance

The LPDDR2 interface fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3 interface fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 37 shows DDR I/O output buffer impedance of i.MX 6Dual/6Quad processors.

Table 37. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	Drive Strength (DSE) =			Ω
		000	Hi-Z	Hi-Z	
		001	240	240	
		010	120	120	
		011	80	80	
		100	60	60	
		101	48	48	
		110	40	40	
		111	34	34	

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 W external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4.8.3 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

4.9 System Modules Timing

This section contains the timing and electrical parameters for the modules in each i.MX 6Dual/6Quad processor.

CAUTION

The timing values are not updated per the design timing analysis results, and will be subject to thorough validation of the silicon towards qualification.

4.9.1 Reset Timings Parameters

Figure 7 shows the reset timing and Table 38 lists the timing parameters.

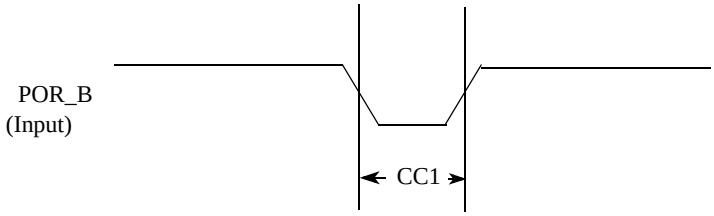


Figure 7. Reset Timing Diagram

Table 38. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid (input slope <= 5 ns)	1	—	T_{CKIL}

4.9.2 WDOG Reset Timing Parameters

Figure 8 shows the WDOG reset timing and Table 39 lists the timing parameters.

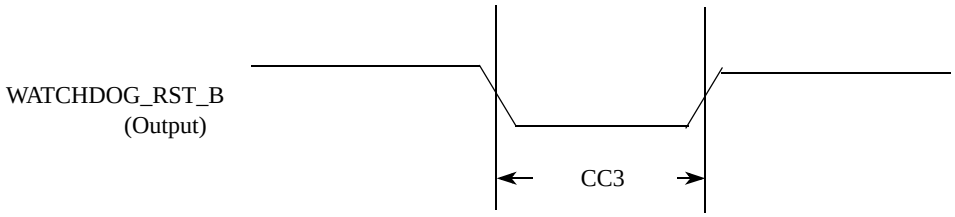


Figure 8. WATCHDOG_RST Timing Diagram

Table 39. WATCHDOG_RST Timing Parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WATCHDOG_RESET Assertion	1	—	T_{CKIL}

NOTE

CKIL is approximately 32 kHz. T_{CKIL} is one period or approximately 30 µs.

NOTE

WATCHDOG_RESET_B output signals (for each one of the Watchdog modules) do not have dedicated bins, but are muxed out through the IOMUX. See the IOMUX manual for detailed information.

4.9.3 External Interface Module (EIM)

The following subsections provide information on the EIM.

4.9.3.1 EIM Signal Cross Reference

Table 40 is a guide intended to help the user identify signals in the External Interface Module chapter of the reference manual that are identical to those mentioned in this data sheet.

Table 40. EIM Signal Cross Reference

Reference Manual EIM Chapter Nomenclature	Data Sheet Nomenclature, Reference Manual External Signals and Pin Multiplexing Chapter, and IOMUXC Controller Chapter Nomenclature
BCLK	EIM_BCLK
CSx	EIM_CSx

Table 40. EIM Signal Cross Reference (continued)

Reference Manual EIM Chapter Nomenclature	Data Sheet Nomenclature, Reference Manual External Signals and Pin Multiplexing Chapter, and IOMUXC Controller Chapter Nomenclature
WE_B	EIM_RW
OE_B	EIM_OE
BEy_B	EIM_EBx
ADV	EIM_LBA
ADDR	EIM_A[25:16], EIM_DA[15:0]
ADDR/M_DATA	EIM_DAx (Addr/Data muxed mode)
DATA	EIM_NFC_D (Data bus shared with NAND Flash) EIM_Dx (dedicated data bus)
WAIT_B	EIM_WAIT

4.9.3.2 EIM Interface Pads Allocation

EIM supports 32-bit, 16-bit and 8-bit devices operating in address/data separate or multiplexed modes. Table 41 provides EIM interface pads allocation in different modes.

Table 41. EIM Internal Module Multiplexing

Setup	Non Multiplexed Address/Data Mode							Multiplexed Address/Data mode	
	8 Bit				16 Bit		32 Bit	16 Bit	32 Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 110	MUM = 0, DSZ = 111	MUM = 0, DSZ = 001	MUM = 0, DSZ = 010	MUM = 0, DSZ = 011	MUM = 1, DSZ = 010	MUM = 1, DSZ = 011
A[15:0]	WEIM_DA_A [15:0]	WEIM_DA_A [15:0]	WEIM_DA_A [15:0]	WEIM_DA_A [15:0]	WEIM_DA_A [15:0]	WEIM_DA_A [15:0]	WEIM_DA_A [15:0]	WEIM_DA_A [15:0]	WEIM_DA_A [15:0]
A[25:16]	WEIM_A [25:16]	WEIM_A [25:16]	WEIM_A [25:16]	WEIM_A [25:16]	WEIM_A [25:16]	WEIM_A [25:16]	WEIM_A [25:16]	WEIM_A [25:16]	WEIM_A [25:16]
D[7:0], EIM_EB0	WEIM_D [7:0]	—		—	WEIM_D [7:0]	—	WEIM_D [7:0]	WEIM_DA_A [7:0]	WEIM_DA_A [7:0]
D[15:8], EIM_EB1	—	WEIM_D [15:8]		—	WEIM_D [15:8]	—	WEIM_D [15:8]	WEIM_DA_A [15:8]	WEIM_DA_A [15:8]
D[23:16], EIM_EB2	—	—	WEIM_D [24:16]	—	—	WEIM_D [23:16]	EIM_D[23:16]	—	WEIM_D [23:16]
D[31:24], EIM_EB3	—	—		WEIM_D [31:24]	—	WEIM_D [31:24]	EIM_D[31:24]	—	WEIM_D [31:24]

4.9.3.3 General EIM Timing-Synchronous Mode

Figure 9, Figure 10, and Table 42 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the BCLK rising edge according to corresponding assertion/negation control fields.

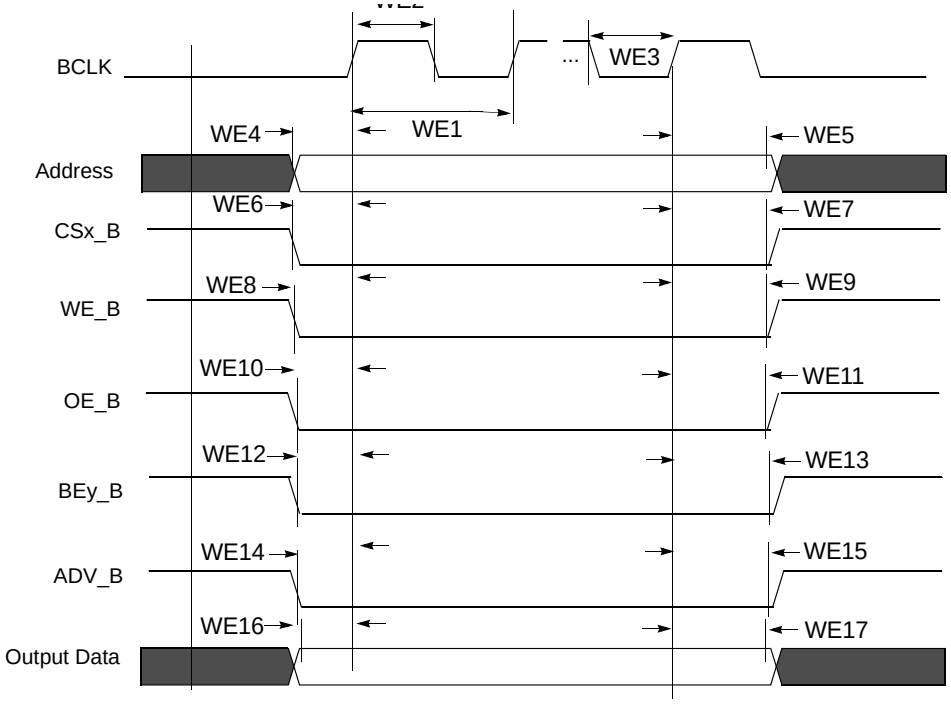


Figure 9. EIM Outputs Timing Diagram

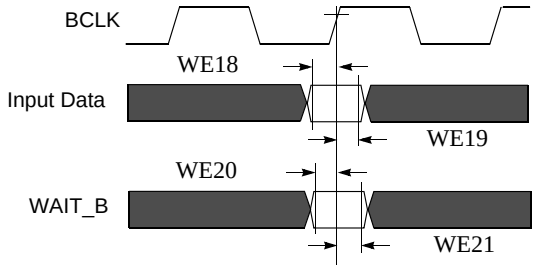


Figure 10. EIM Inputs Timing Diagram

4.9.3.4 Examples of EIM Synchronous Accesses

Table 42. EIM Bus Timing Parameters [1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE1	BCLK Cycle time[2]	t	—	2*t		3*t	—	4*t	—
WE2	BCLK Low Level Width	0.4*t	—	0.8*t		1.2*t	—	1.6*t	—
WE3	BCLK High Level Width	0.4*t	—	0.8*t		1.2*t	—	1.6*t	—
WE4	Clock rise to address valid[3]	-0.5*t-1.25	-0.5*t+1.75	-t-1.25	-t+1.75	-1.5*t-1.25	-1.5*t +1.75	-2*t-1.25	-2*t+1.75
WE5	Clock rise to address invalid	0.5*t-1.25	0.5*t+1.75	t-1.25	t+1.75	1.5*t-1.25	1.5*t +1.75	2*t-1.25	2*t+1.75
WE6	Clock rise to CSx_B valid	-0.5*t-1.25	-0.5*t+1.75	-t-1.25	-t+1.75	-1.5*t-1.25	-1.5*t +1.75	-2*t-1.25	-2*t+1.75
WE7	Clock rise to CSx_B invalid	0.5*t-1.25	0.5*t+1.75	t-1.25	t+1.75	1.5*t-1.25	1.5*t +1.75	2*t-1.25	2*t+1.75
WE8	Clock rise to WE_B Valid	-0.5*t-1.25	-0.5*t+1.75	-t-1.25	-t+1.75	-1.5*t-1.25	-1.5*t +1.75	-2*t-1.25	-2*t+1.75
WE9	Clock rise to WE_B Invalid	0.5*t-1.25	0.5*t+1.75	t-1.25	t+1.75	1.5*t-1.25	1.5*t +1.75	2*t-1.25	2*t+1.75
WE10	Clock rise to OE_B Valid	-0.5*t-1.25	-0.5*t+1.75	-t-1.25	-t+1.75	-1.5*t-1.25	-1.5*t +1.75	-2*t-1.25	-2*t+1.75
WE11	Clock rise to OE_B Invalid	0.5*t-1.25	0.5*t+1.75	t-1.25	t+1.75	1.5*t-1.25	1.5*t +1.75	2*t-1.25	2*t+1.75
WE12	Clock rise to BEy_B Valid	-0.5*t-1.25	-0.5*t+1.75	-t-1.25	-t+1.75	-1.5*t-1.25	-1.5*t +1.75	-2*t-1.25	-2*t+1.75
WE13	Clock rise to BEy_B Invalid	0.5*t-1.25	0.5*t+1.75	t-1.25	t+1.75	1.5*t-1.25	1.5*t +1.75	2*t-1.25	2*t+1.75
WE14	Clock rise to ADV_B Valid	-0.5*t-1.25	-0.5*t+1.75	-t-1.25	-t+1.75	-1.5*t-1.25	-1.5*t +1.75	-2*t-1.25	-2*t+1.75
WE15	Clock rise to ADV_B Invalid	0.5*t-1.25	0.5*t+1.75	t-1.25	t+1.75	1.5*t-1.25	1.5*t +1.75	2*t-1.25	2*t+1.75
WE16	Clock rise to Output Data Valid	-0.5*t-1.25	-0.5*t+1.75	-t-1.25	-t+1.75	-1.5*t-1.25	-1.5*t +1.75	-2*t-1.25	-2*t+1.75
WE17	Clock rise to Output Data Invalid	0.5*t-1.25	0.5*t+1.75	t-1.25	t+1.75	1.5*t-1.25	1.5*t +1.75	2*t-1.25	2*t+1.75
WE18	Input Data setup time to Clock rise	2	—	4	—	—	—	—	—

Table 42. EIM Bus Timing Parameters (continued)[1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE19	Input Data hold time from Clock rise	2	—	2	—	—	—	—	—
WE20	WAIT_B setup time to Clock rise	2	—	4	—	—	—	—	—
WE21	WAIT_B hold time from Clock rise	2	—	2	—	—	—	—	—

1 t is the maximal EIM logic (axi_clk) cycle time. The maximum allowed axi_clk frequency depends on the fixed/non-fixed latency configuration, whereas the maximum allowed BCLK frequency is:

—Fixed latency for both read and write is 132 MHz.

—Variable latency for read only is 132 MHz.

—Variable latency for write only is 52 MHz.

In variable latency configuration for write, if BCD = 0 & WBCDD = 1 or BCD = 1, axi_clk must be 104 MHz.Write BCD = 1 and 104 MHz axi_clk, will result in a BCLK of 52 MHz. When the clock branch to EIM is decreased to 104 MHz, other buses are impacted which are clocked from this source. See the CCM chapter of the i.MX 6Dual/6Quad reference manual for a detailed clock tree description.

2 BCLK parameters are being measured from the 50% point, that is, high is defined as 50% of signal value and low is defined as 50% as signal value.

3 For signal measurements, “High” is defined as 80% of signal value and “Low” is defined as 20% of signal value.

Figure 11 to Figure 14 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

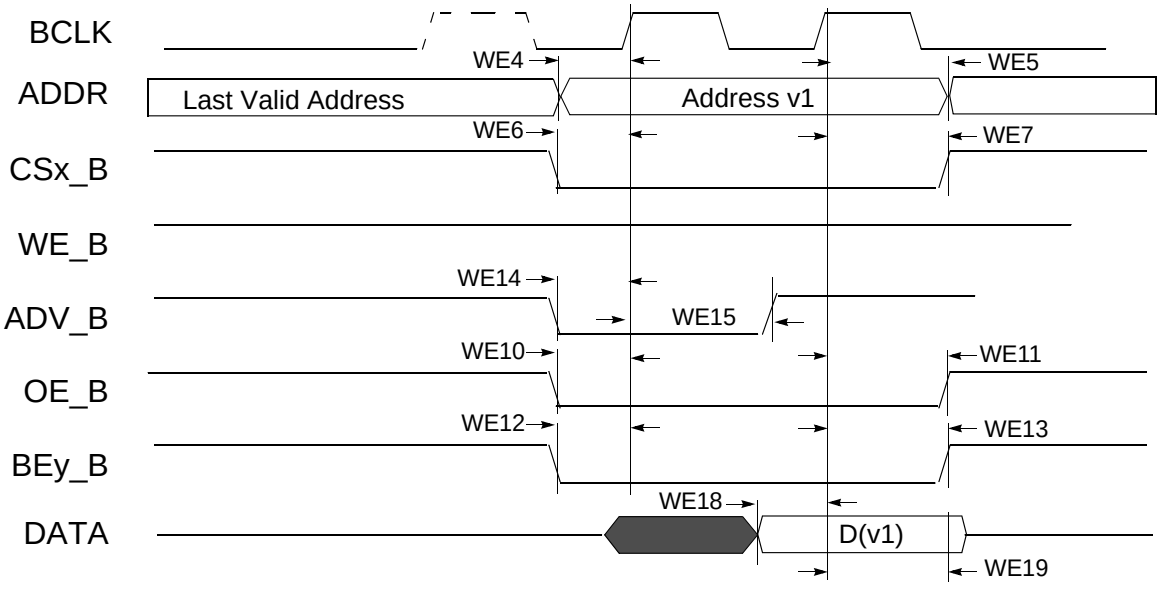


Figure 11. Synchronous Memory Read Access, WSC=1

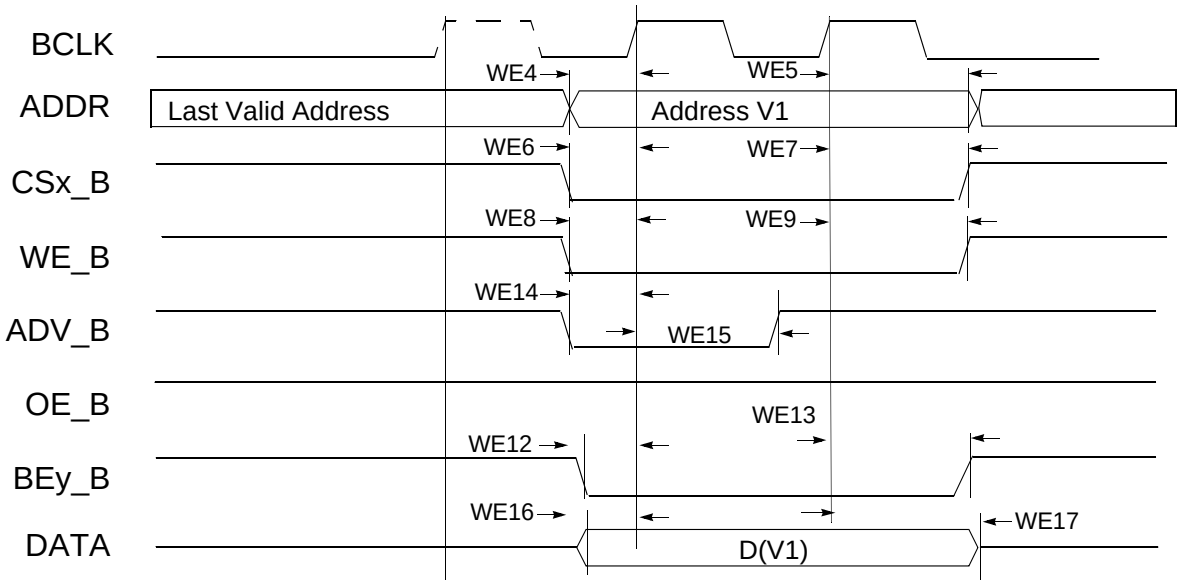


Figure 12. Synchronous Memory, Write Access, WSC=1, WBEA=0 and WADVN=0

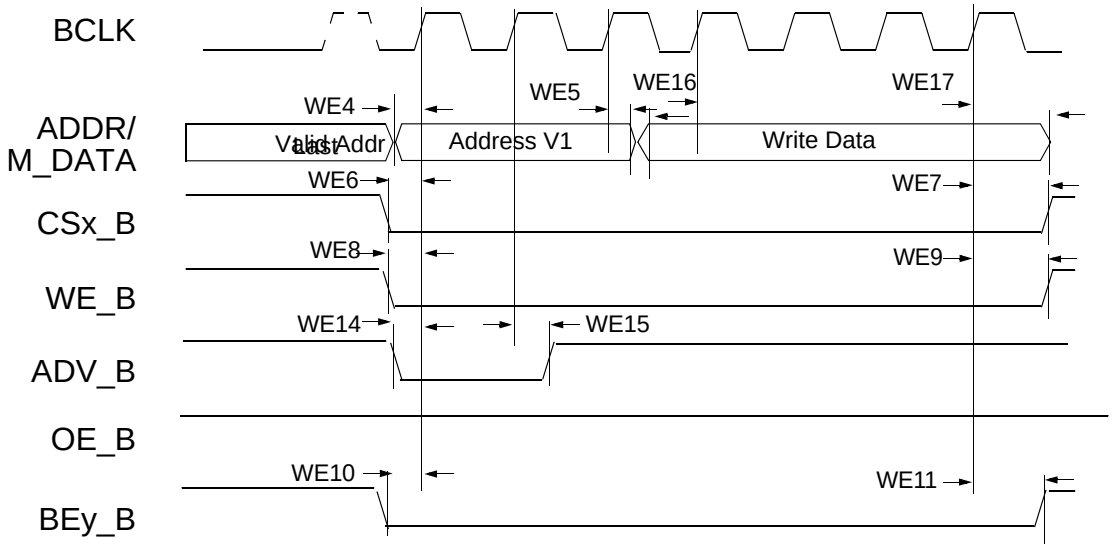


Figure 13. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6,ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

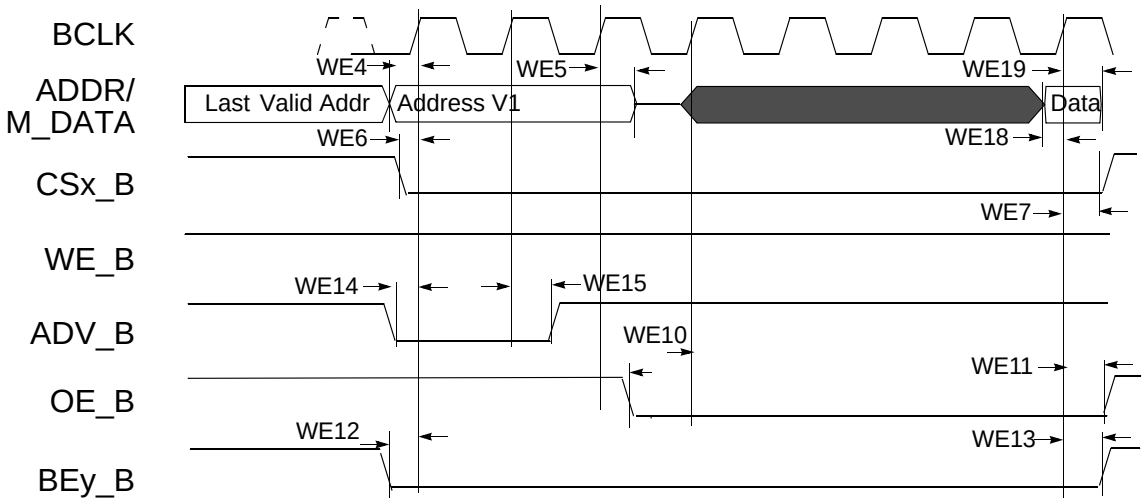


Figure 14. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

4.9.3.5 General EIM Timing-Asynchronous Mode

Figure 15 through Figure 19, and Table 43 help you determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read & write access length in cycles may vary from what is shown in Figure 15 through Figure 18 as RWSC, OEN & CSN is configured differently. See the i.MX 6Dual/6Quad reference manual for the EIM programming model.

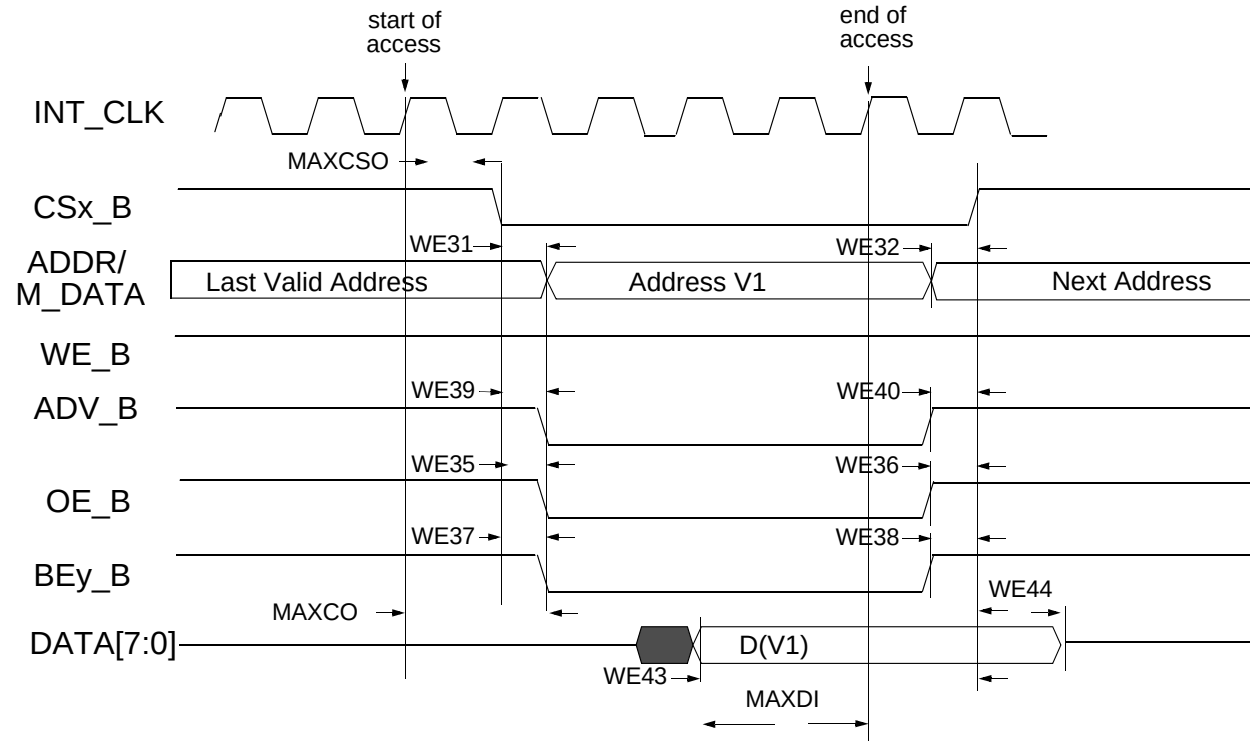


Figure 15. Asynchronous Memory Read Access (RWSC = 5)

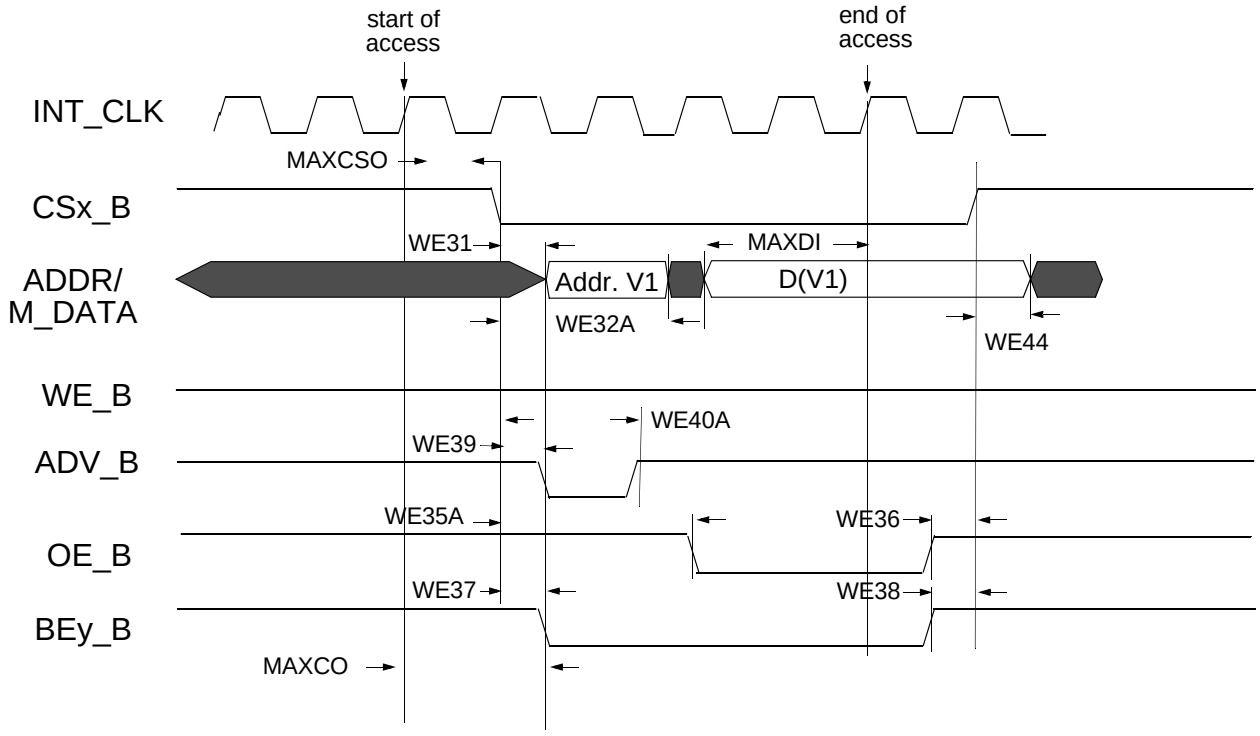


Figure 16. Asynchronous A/D Muxed Read Access (RWSC = 5)

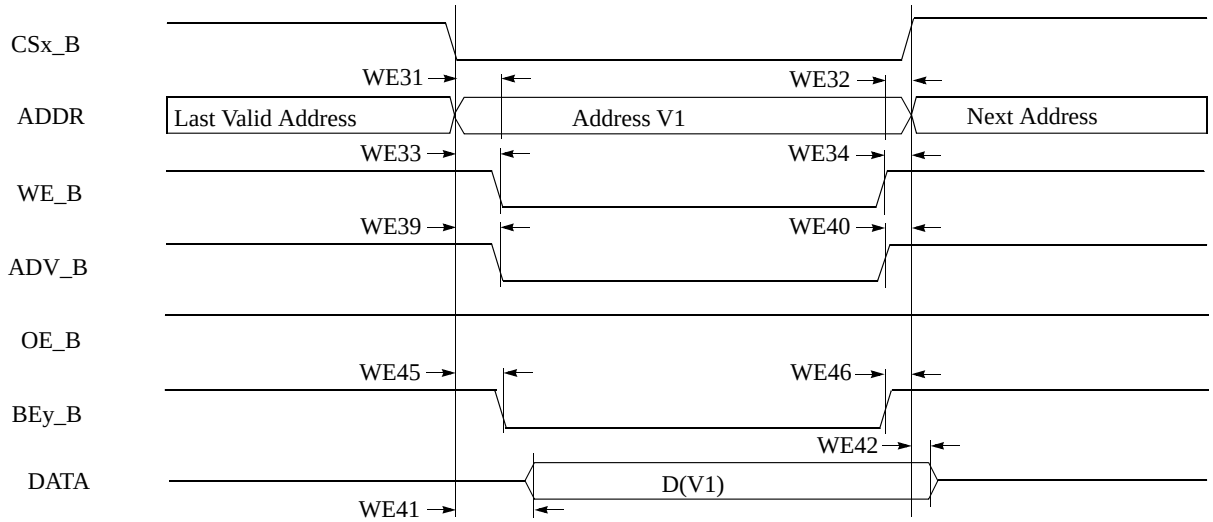


Figure 17. Asynchronous Memory Write Access

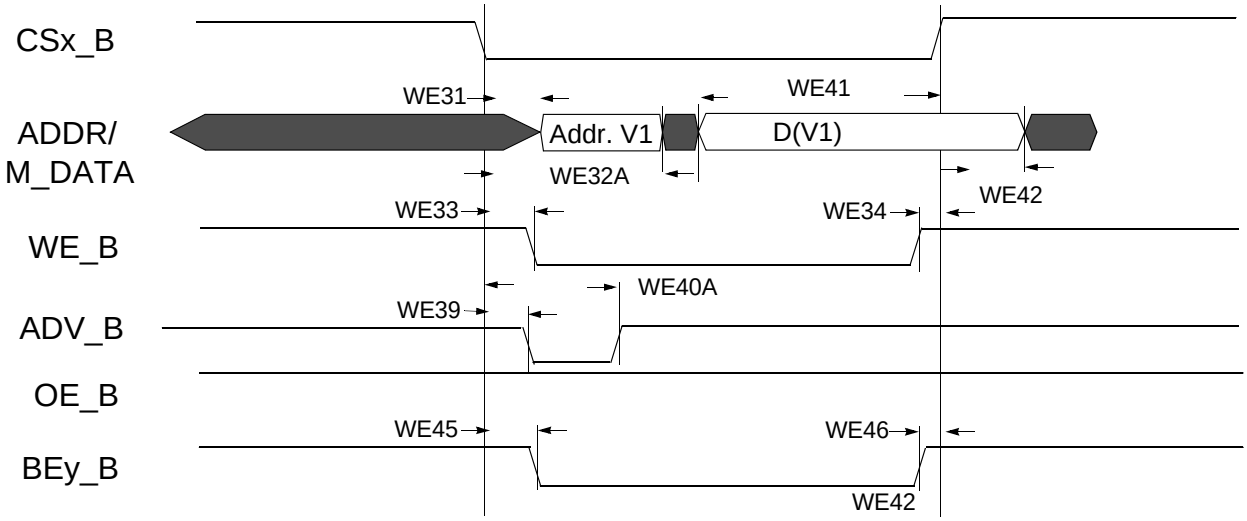


Figure 18. Asynchronous A/D Muxed Write Access

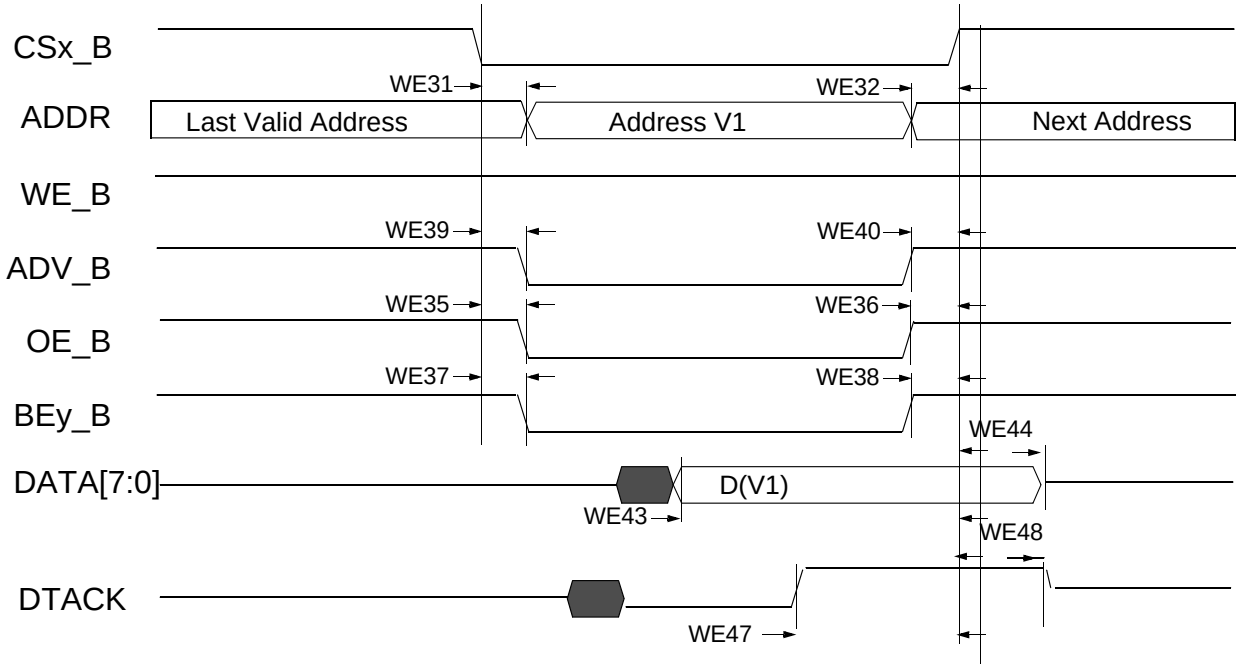


Figure 19. DTACK Read Access (DAP=0)

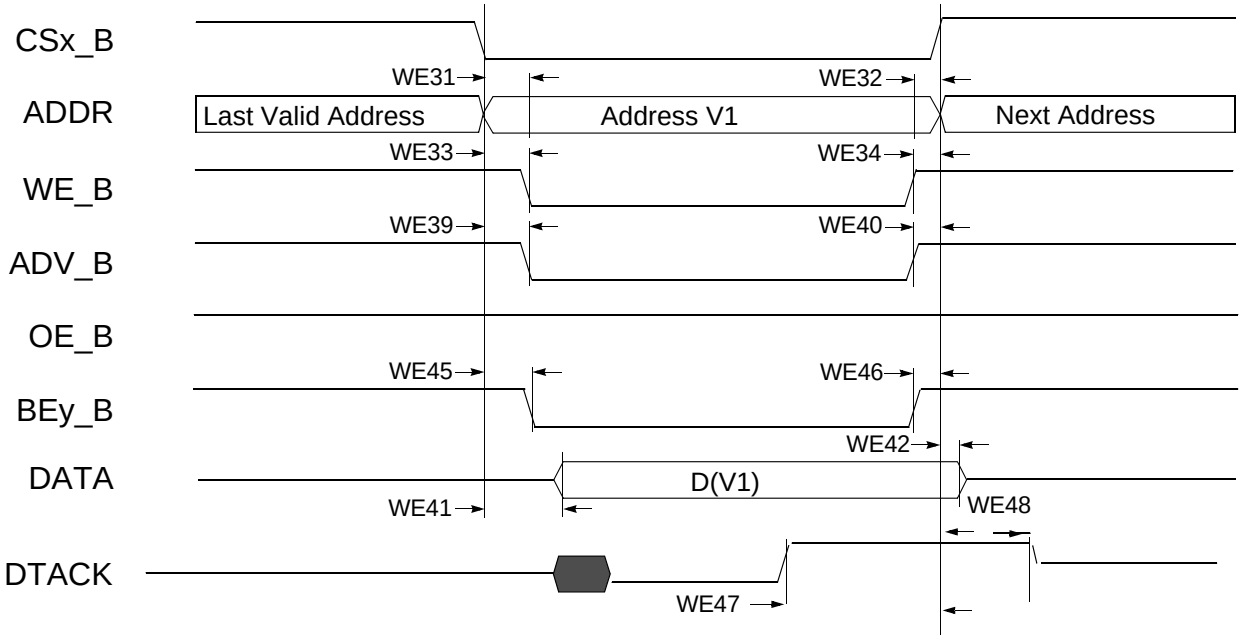


Figure 20. DTACK Write Access (DAP=0)

Table 43. EIM Asynchronous Timing Parameters Table Relative Chip Select

Ref No.	Parameter	Determination by Synchronous measured parameters[12]	Min	Max (If 132 MHz is supported by SOC)	Unit
WE31	CSx_B valid to Address Valid	WE4 - WE6 - CSA[3]	—	3 - CSA	ns
WE32	Address Invalid to CSx_B invalid	WE7 - WE5 - CSN[4]	—	3 - CSN	ns
WE32A(muxed A/D	CSx_B valid to Address Invalid	t[5] + WE4 - WE7 + (ADVN + ADVA + 1 - CSA[3])	-3 + (ADVN + ADVA + 1 - CSA)	—	ns
WE33	CSx_B Valid to WE_B Valid	WE8 - WE6 + (WEA - CSA)	—	3 + (WEA - CSA)	ns
WE34	WE_B Invalid to CSx_B Invalid	WE7 - WE9 + (WEN - CSN)	—	3 - (WEN_CSN)	ns
WE35	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA - CSA)	—	3 + (OEA - CSA)	ns
WE35A (muxed A/D)	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA + RADVN + RADVA + ADH + 1 - CSA)	-3 + (OEA + RADVN+RADVA+ ADH+1-CSA)	3 + (OEA + RADVN+RADVA+AD H+1-CSA)	ns
WE36	OE_B Invalid to CSx_B Invalid	WE7 - WE11 + (OEN - CSN)	—	3 - (OEN - CSN)	ns
WE37	CSx_B Valid to BEy_B Valid (Read access)	WE12 - WE6 + (RBEA - CSA)	—	3 + (RBEA[6] - CSA)	ns
WE38	BEy_B Invalid to CSx_B Invalid (Read access)	WE7 - WE13 + (RBEN - CSN)	—	3 - (RBEN[7]- CSN)	ns
WE39	CSx_B Valid to ADV_B Valid	WE14 - WE6 + (ADVA - CSA)	—	3 + (ADVA - CSA)	ns
WE40	ADV_B Invalid to CSx_B Invalid (ADVL is asserted)	WE7 - WE15 - CSN	—	3 - CSN	ns
WE40A (muxed A/D)	CSx_B Valid to ADV_B Invalid	WE14 - WE6 + (ADVN + ADVA + 1 - CSA)	-3 + (ADVN + ADVA + 1 - CSA)	3 + (ADVN + ADVA + 1 - CSA)	ns
WE41	CSx_B Valid to Output Data Valid	WE16 - WE6 - WCSA	—	3 - WCSA	ns
WE41A (muxed A/D)	CSx_B Valid to Output Data Valid	WE16 - WE6 + (WADVN + WADVA + ADH + 1 - WCSA)	—	3 + (WADVN + WADVA + ADH + 1 - WCSA)	ns
WE42	Output Data Invalid to CSx_B Invalid	WE17 - WE7 - CSN	—	3 - CSN	ns
MAXCO	Output max. delay from internal driving ADDR/control FFs to chip outputs.	10	—	—	ns
MAXCS O	Output max. delay from CSx internal driving FFs to CSx out.	10	—	—	
MAXDI	DATA MAXIMUM delay from chip input data to its internal FF	5	—	—	

Table 43. EIM Asynchronous Timing Parameters Table Relative Chip Select (continued)

Ref No.	Parameter	Determination by Synchronous measured parameters[12]	Min	Max (If 132 MHz is supported by SOC)	Unit
WE43	Input Data Valid to CSx_B Invalid	MAXCO - MAXCSO + MAXDI	MAXCO - MAXCSO + MAXDI	—	ns
WE44	CSx_B Invalid to Input Data invalid	0	0	—	ns
WE45	CSx_B Valid to BEy_B Valid (Write access)	WE12 - WE6 + (WBEA - CSA)	—	3 + (WBEA - CSA)	ns
WE46	BEy_B Invalid to CSx_B Invalid (Write access)	WE7 - WE13 + (WBEN - CSN)	—	-3 + (WBEN - CSN)	ns
MAXDTI	DTACK MAXIMUM delay from chip dtack input to its internal FF + 2 cycles for synchronization	10	—	—	ns
WE47	Dtack Active to CSx_B Invalid	MAXCO - MAXCSO + MAXDTI	MAXCO - MAXCSO + MAXDTI	—	ns
WE48	CSx_B Invalid to Dtack invalid	0	0	—	ns

1 Parameters WE4... WE21 value see column BCD = 0 in Table 42.

2 All configuration parameters (CSA, CSN, WBEA, WBEN, ADVA, ADVN, OEN, OEA, RBEA, and RBEN) are in cycle units.

3 CS Assertion. This bit field determines when CS signal is asserted during read/write cycles.

4 CS Negation. This bit field determines when CS signal is negated during read/write cycles.

5 t is axi_clk cycle time.

6 BE Assertion. This bit field determines when BE signal is asserted during read cycles.

7 BE Negation. This bit field determines when BE signal is negated during read cycles.

4.9.4 DDR SDRAM Specific Parameters (DDR3 and LPDDR2)

4.9.4.1 DDR3 Parameters

Figure 21 shows the basic timing parameters. The timing parameters for this diagram appear in Table 44.

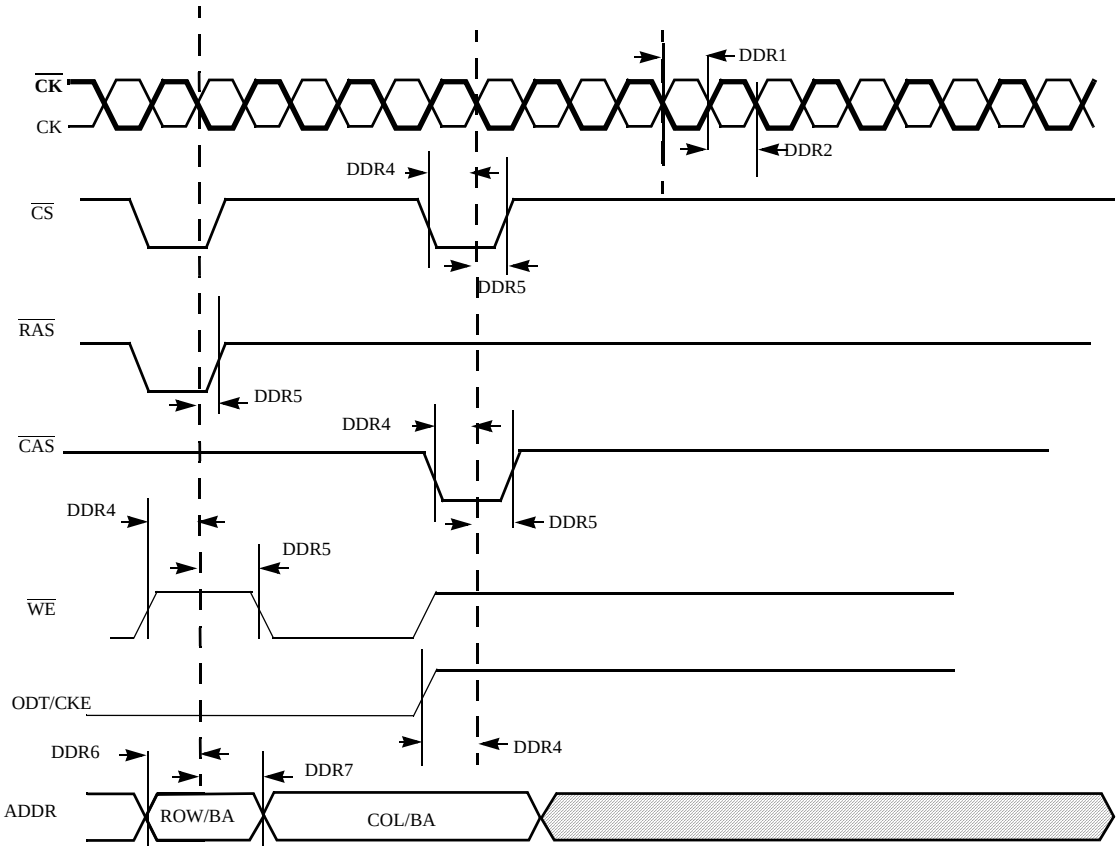


Figure 21. DDR3 Command and Address Timing Parameters

Table 44. DDR3 Timing Parameter Table

ID	Parameter	Symbol	CK = 532 MHz		Unit
			Min	Max	
DDR1	CK clock high-level width	t_{CH}	0.47	0.53	t_{CK}
DDR2	CK clock low-level width	t_{CL}	0.47	0.53	t_{CK}
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	t_{IS}	440	—	ps
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	t_{IH}	315	—	ps
DDR6	Address output setup time	t_{IS}	440	—	ps
DDR7	Address output hold time	t_{IH}	315	—	ps

1 All measurements are in reference to Vref level.

2 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

Figure 22shows the write timing parameters. The timing parameters for this diagram appear in Table 45.

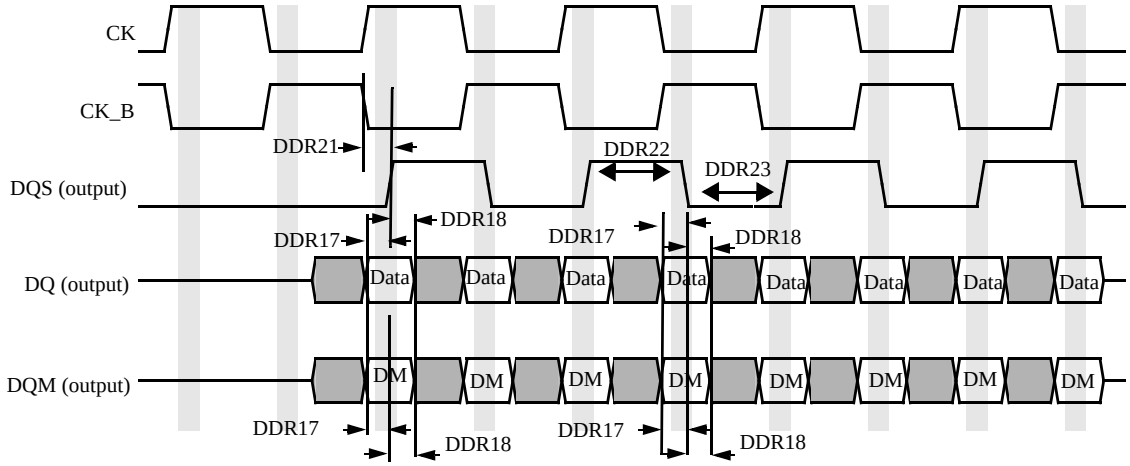


Figure 22. DDR3 Write Cycle

Table 45. DDR3 Write Cycle

ID	Parameter	Symbol	CK = 532 MHz		Unit
			Min	Max	
DDR17	DQ and DQM setup time to DQS (differential strobe)	t_{DS}	240	—	ps
DDR18	DQ and DQM hold time to DQS (differential strobe)	t_{DH}	215	—	ps
DDR21	DQS latching rising transitions to associated clock edges	t_{DQSS}	-0.25	+0.25	tCK
DDR22	DQS high level width	t_{DQSH}	0.45	0.55	tCK
DDR23	DQS low level width	t_{DQSL}	0.45	0.55	tCK

1 To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

2 All measurements are in reference to Vref level.

3 Measurements were done using balanced load and 25 W resistor from outputs to VDD_REF.

Figure 23 shows the read timing parameters. The timing parameters for this diagram appear in Table 46.

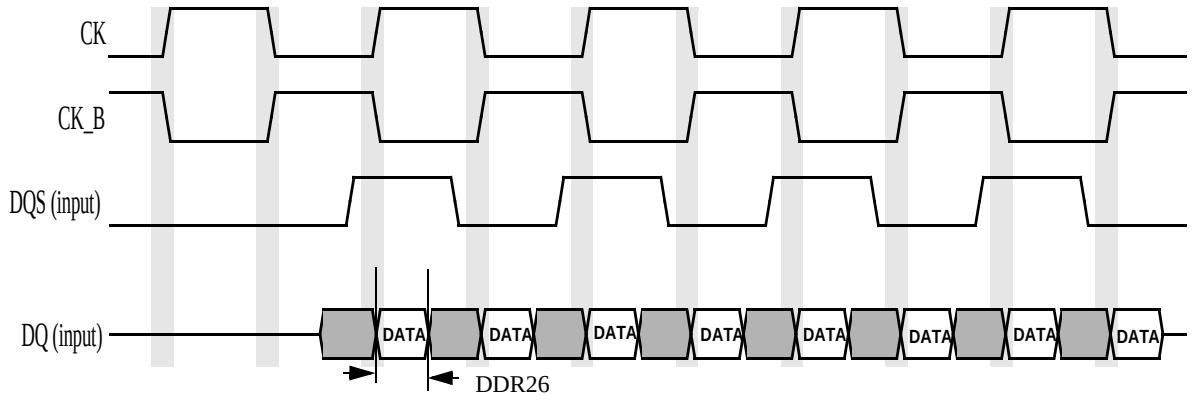


Figure 23. DDR3 Read Cycle

Table 46. DDR3 Read Cycle

ID	Parameter	Symbol	CK = 532 MHz		Unit
			Min	Max	
DDR26	Minimum required DQ valid window width	—	550	—	ps

1 To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

2 All measurements are in reference to Vref level.

3 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

4.9.4.2 LPDDR2 Parameters

Figure 24 shows the basic timing parameters. The timing parameters for this diagram appear in Table 47.

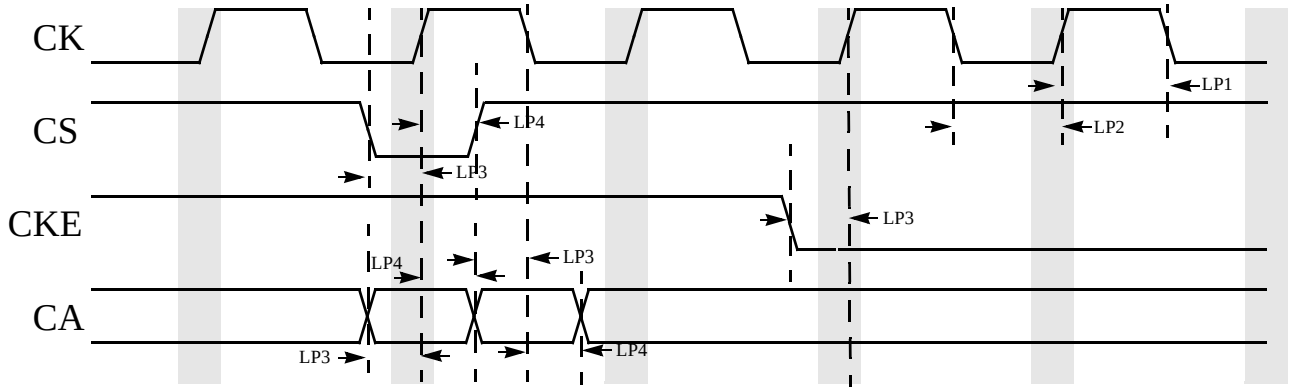


Figure 24. LPDDR2 Command and Address Timing Parameters

Table 47. LPDDR2 Timing Parameter

ID	Parameter	Symbol	CK = 532 MHz		Unit
			Min	Max	
LP1	SDRAM clock high-level width	t_{CH}	0.45	0.55	t_{CK}
LP2	SDRAM clock low-level width	t_{CL}	0.45	0.55	t_{CK}
LP3	CS, CKE setup time	t_{IS}	230	—	ps
LP4	CS, CKE hold time	t_{IH}	230	—	ps
LP3	CA setup time	t_{IS}	230	—	ps
LP4	CA hold time	t_{IH}	230	—	ps

1 All measurements are in reference to Vref level.
2 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

Figure 25 shows the write timing parameters. The timing parameters for this diagram appear in Table 48.

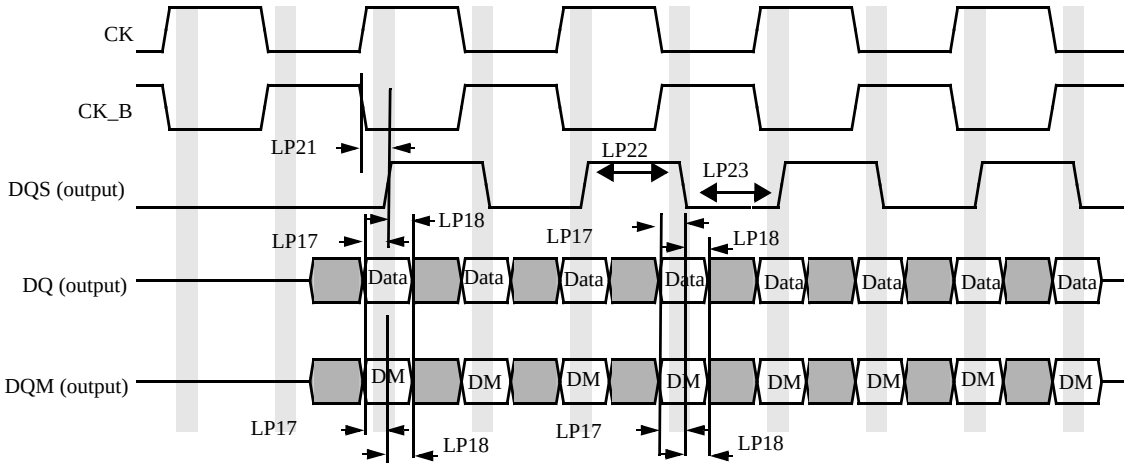


Figure 25. LPDDR2 Write Cycle

Table 48. LPDDR2 Write Cycle

ID	Parameter	Symbol	CK = 532 MHz		Unit
			Min	Max	
LP17	DQ and DQM setup time to DQS (differential strobe)	t_{DS}	220	—	ps
LP18	DQ and DQM hold time to DQS (differential strobe)	t_{DH}	220	—	ps
LP21	DQS latching rising transitions to associated clock edges	t_{DQSS}	-0.25	+0.25	tCK
LP22	DQS high level width	t_{DQSH}	0.4	-	tCK
LP23	DQS low level width	t_{DQSL}	0.4	-	tCK

1 To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

2 All measurements are in reference to Vref level.

3 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

Figure 26 shows the read timing parameters. The timing parameters for this diagram appear in Table 49.

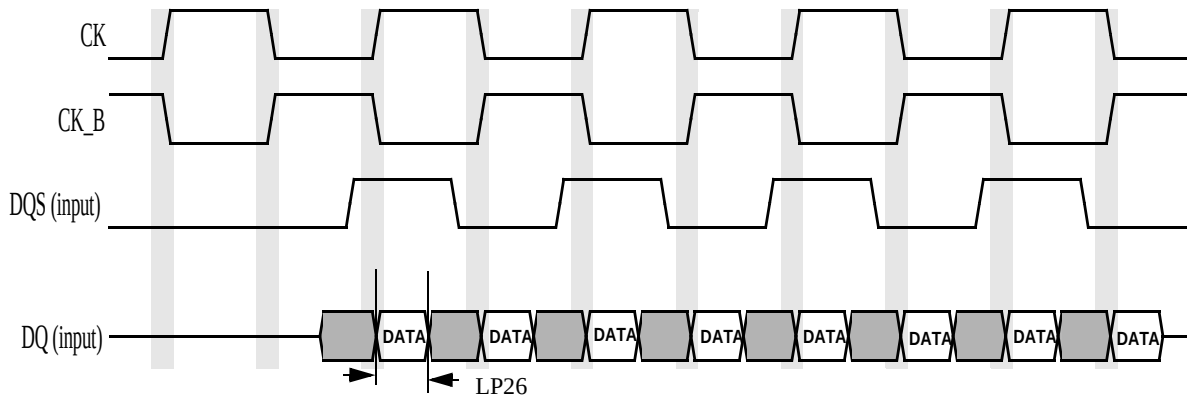


Figure 26. LPDDR2 Read Cycle

Table 49. LPDDR2 Read Cycle

ID	Parameter	Symbol	CK = 532 MHz		Unit
			Min	Max	
LP26	Minimum required DQ valid window width for LPDDR2	—	270	—	ps

1 To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

2 All measurements are in reference to Vref level.

3 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

4.10 General-Purpose Media Interface (GPMI) Timing

The i.MX 6Dual/6Quad GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select.

It supports Asynchronous timing mode, Source Synchronous timing mode and Samsung Toggle timing mode separately described in the following paragraphs.

4.10.1 Asynchronous Mode AC Timing (ONFI 1.0 Compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The maximum I/O speed of GPMI in asynchronous mode is about 50 MB/s. Figure 27 through Figure 30 depicts the relative timing between GPMI signals at the module level for different operations under asynchronous mode. Table 50 describes the timing parameters (NF1–NF17) that are shown in the figures.

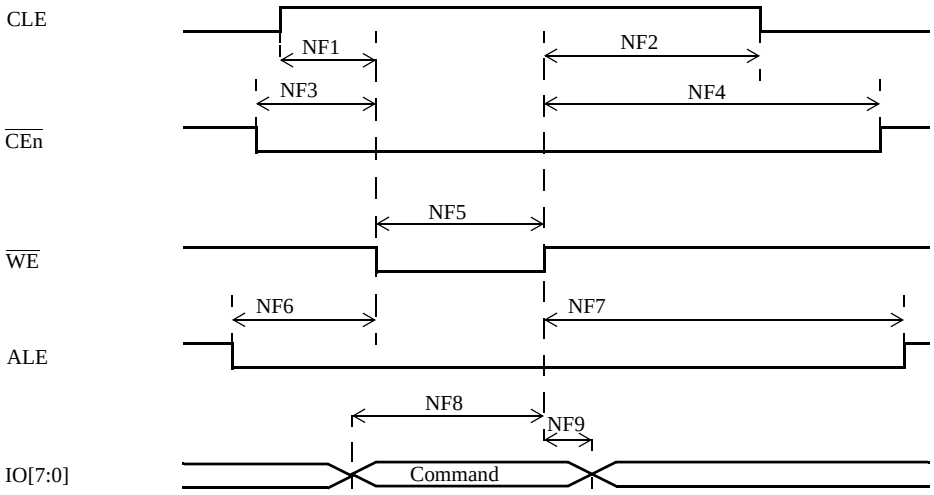


Figure 27. Command Latch Cycle Timing Diagram

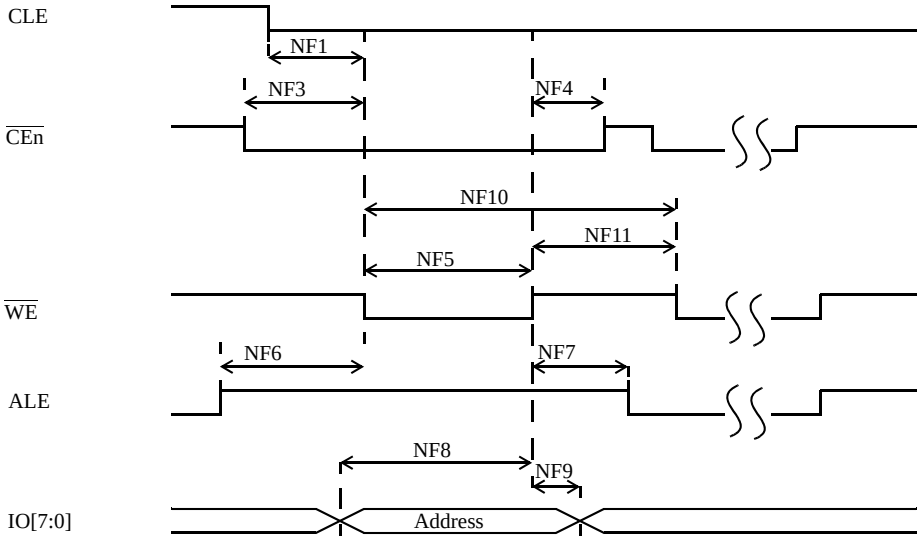


Figure 28. Address Latch Cycle Timing Diagram

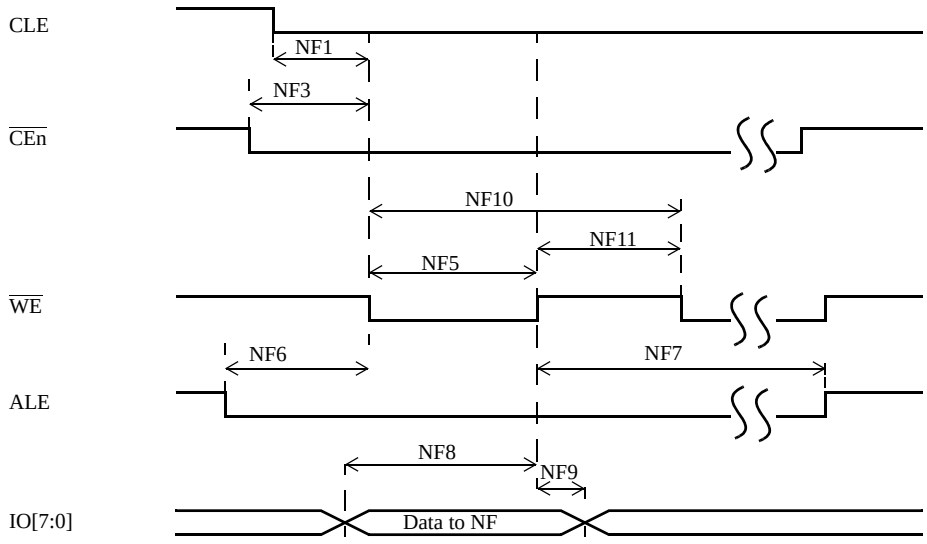


Figure 29. Write Data Latch Cycle Timing Diagram

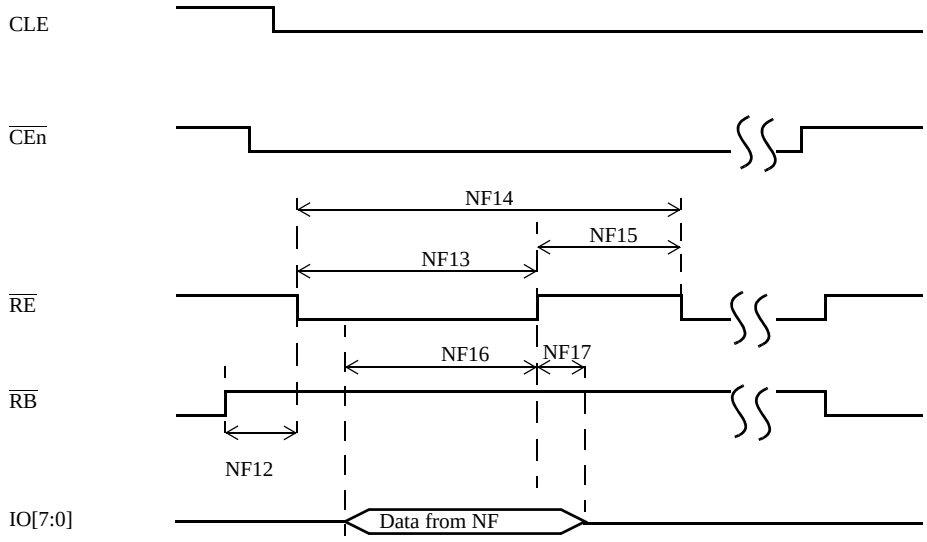


Figure 30. Read Data Latch Cycle Timing Diagram

Table 50. Asynchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T[2] = GPMI Clock Cycle		Example Timing for GPMI Clock ≈ 100 MHz T = 10 ns		Unit
			Min.	Max.	Min.	Max.	
NF1	CLE setup time	tCLS	(AS[3]+1)*T	—	10	—	ns
NF2	CLE hold time	tCLH	(DH+1)*T	—	20	—	ns
NF3	$\overline{\text{CE}}$n setup time	tCS	(AS+1)*T	—	10	—	ns
NF4	$\overline{\text{CE}}$ hold time	tCH	(DH+1)*T	—	20	—	ns

Table 50. Asynchronous Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T[2] = GPMI Clock Cycle		Example Timing for GPMI Clock ≈ 100 MHz T = 10 ns		Unit
			Min.	Max.	Min.	Max.	
NF5	$\overline{WE}$ pulse width	tWP	DS*T		10		ns
NF6	ALE setup time	tALS	(AS+1)*T	—	10	—	ns
NF7	ALE hold time	tALH	(DH+1)*T	—	20	—	ns
NF8	Data setup time	tDS	DS*T	—	10	—	ns
NF9	Data hold time	tDH	DH*T	—	10	—	ns
NF10	Write cycle time	tWC	(DS+DH)*T		20		ns
NF11	$\overline{WE}$ hold time	tWH	DH*T		10		ns
NF12	Ready to $\overline{RE}$ low	tRR	(AS+1)*T	—	10	—	ns
NF13	$\overline{RE}$ pulse width	tRP	DS*T	—	10	—	ns
NF14	READ cycle time	tRC	(DS+DH)*T	—	20	—	ns
NF15	$\overline{RE}$ high hold time	tREH	DH*T		10	—	ns
NF16	Data setup on read	tDSR	N/A		10	—	ns
NF17	Data hold on read	tDHR	N/A		10	—	ns

1 GPMI's Async Mode output timing could be controlled by module's internal registers, say HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers' settings. In the above table, we use AS/DS/DH to represent each of these settings.

2 T represents the GPMI clock period.

3 AS minimum value could be 0, while DS/DH minimum value is 1.

4.10.2 Source Synchronous Mode AC Timing (ONFI 2.x Compatible)

Figure 31 to Figure 33 show the write and read timing of Source Synchronous Mode.

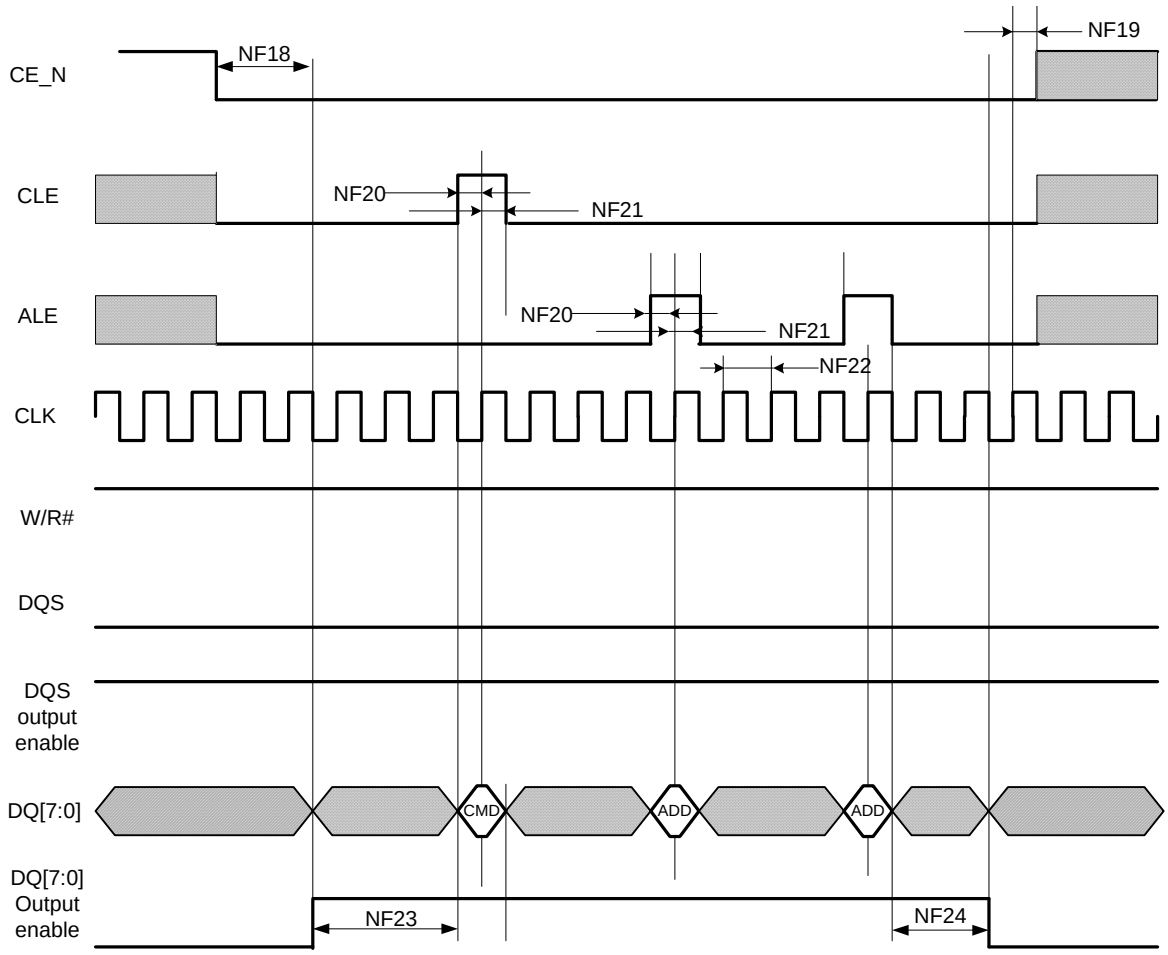


Figure 31. Source Synchronous Mode Command and Address Timing Diagram

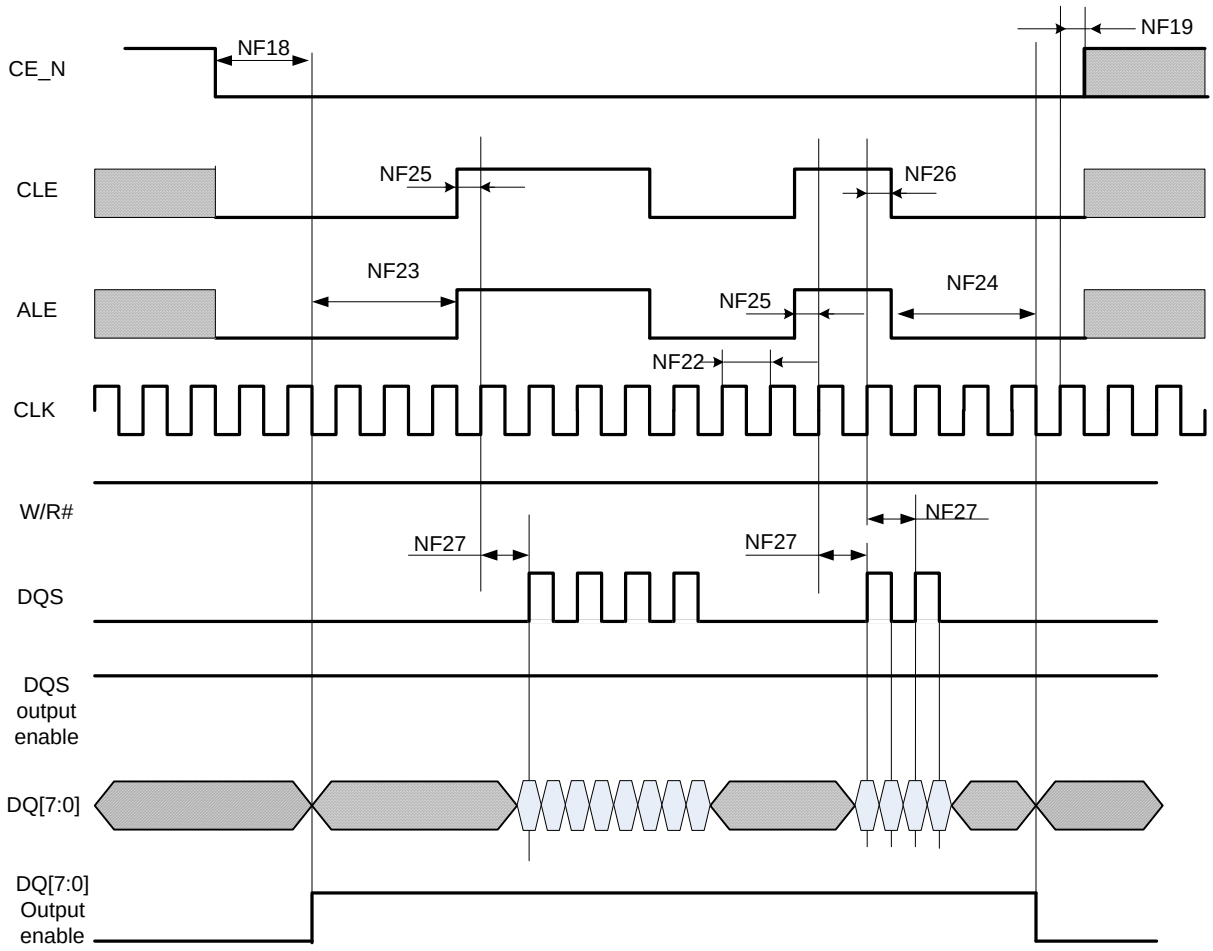


Figure 32. Source Synchronous Mode Data Write Timing Diagram

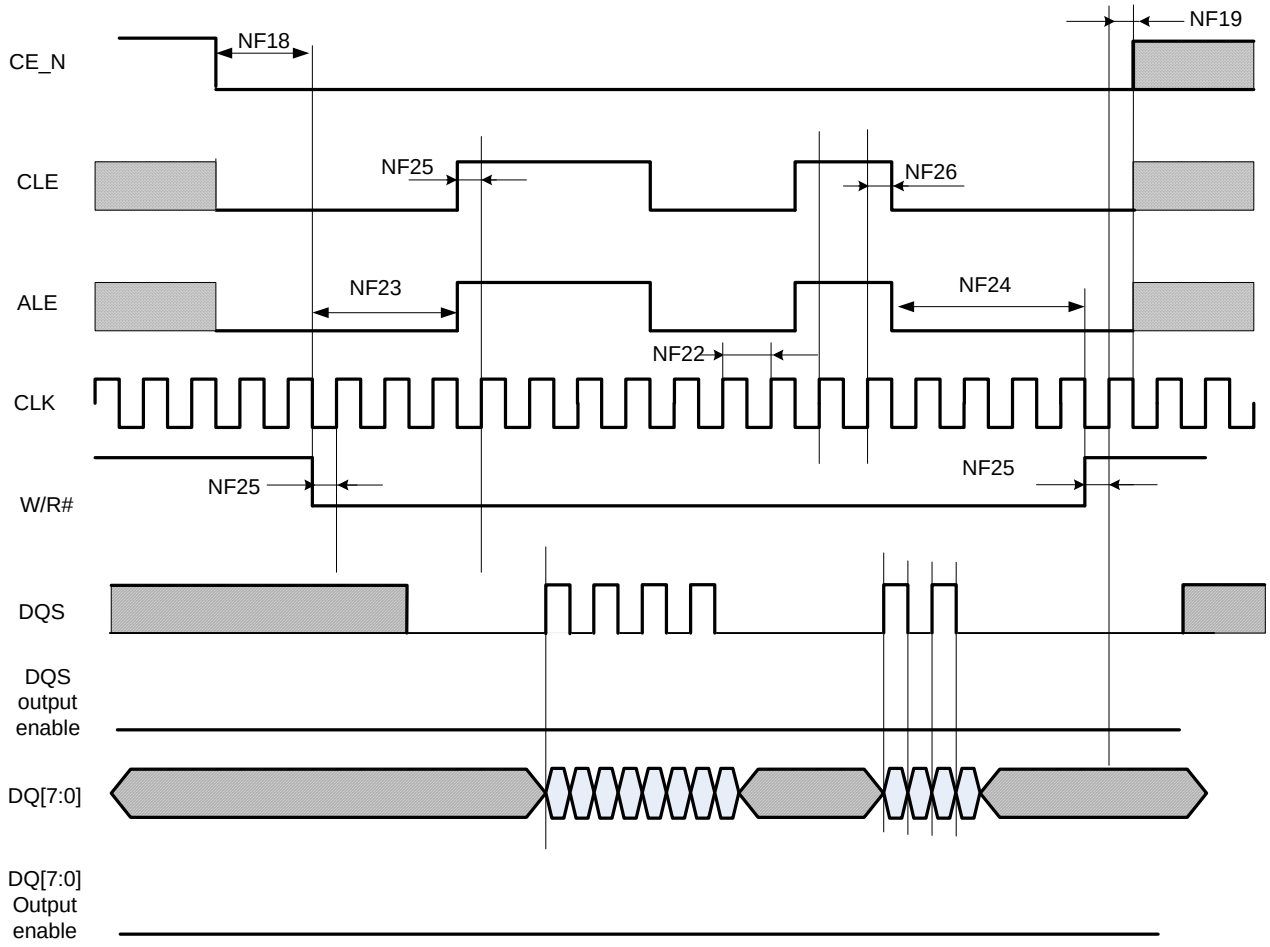


Figure 33. Source Synchronous Mode Data Read Timing Diagram

Table 51. Source Synchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	CE# access time	tCE	CE_DELAY*tCK	—	ns
NF19	CE# hold time	tCH	0.5 *tCK	—	ns
NF20	Command/address DQ setup time	tCAS	0.5*tCK	—	ns
NF21	Command/address DQ hold time	tCAH	0.5*tCK	—	ns
NF22	clock period	tCK	5	--	ns
NF23	preamble delay	tPRE	PRE_DELAY*tCK	—	ns

Table 51. Source Synchronous Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF24	postamble delay	tPOST	POST_DELAY*tCK	—	ns
NF25	CLE and ALE setup time	tCALS	0.5*tCK	—	ns
NF26	CLE and ALE hold time	tCALH	0.5*tCK	—	ns
NF27	Data input to first DQS latching transition	tDQSS	tCK	—	ns

1 GPMI's Sync Mode output timing could be controlled by module's internal registers, say HW_GPMI_TIMING2_CE_DELAY, HW_GPMI_TIMING_PREAMBLE_DELAY, and HW_GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers' settings. In the above table, we use CE_DELAY/PRE_DELAY/POST_DELAY to represent each of these settings.

4.10.3 Samsung Toggle Mode AC Timing

4.10.3.1 Command and Address Timing

NOTE

Samsung Toggle Mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See Section 4.10.1, "Asynchronous Mode AC Timing (ONFI 1.0 Compatible)," for details.

4.10.3.2 Read and Write Timing

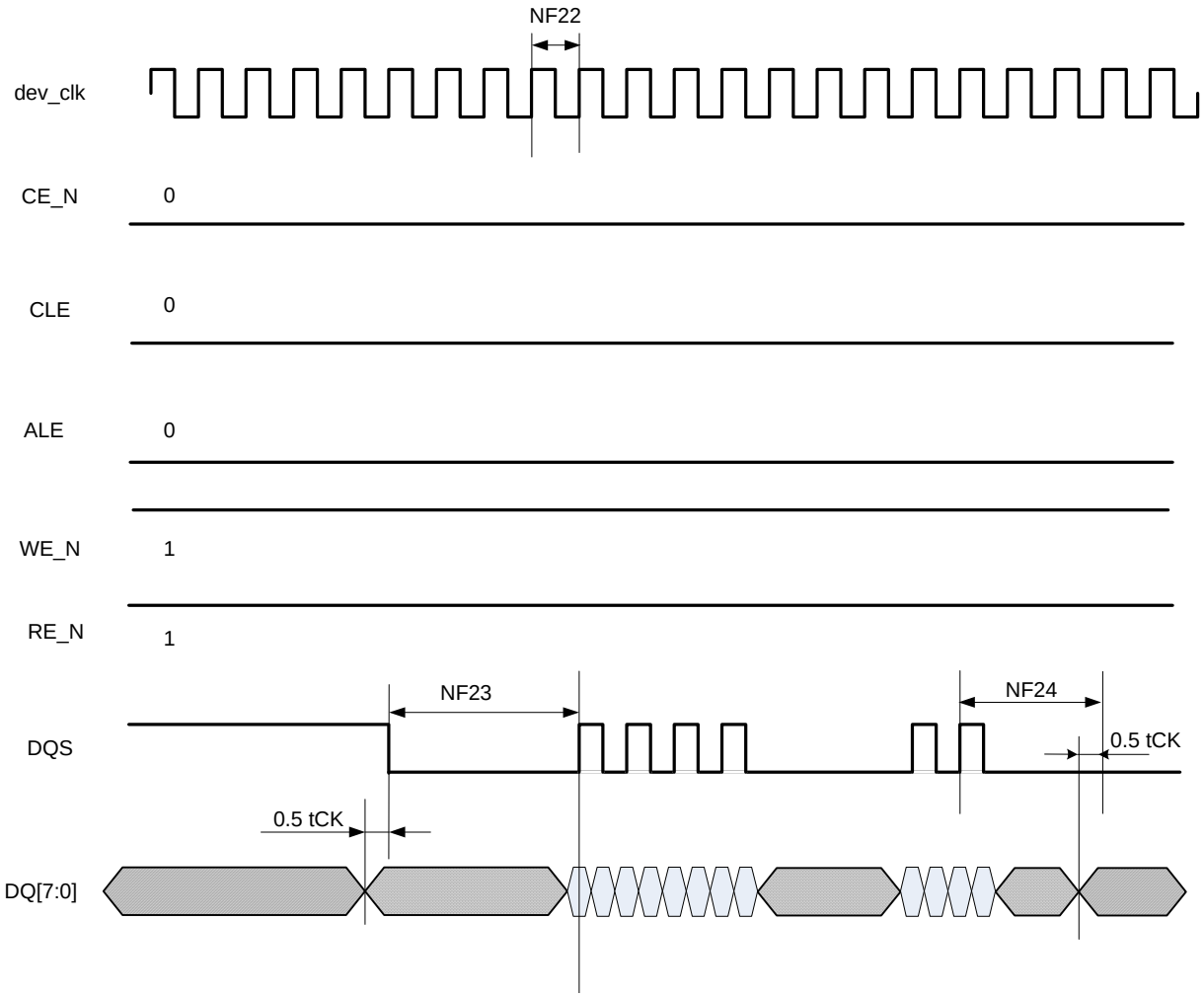


Figure 34. Samsung Toggle Mode Data Write Timing

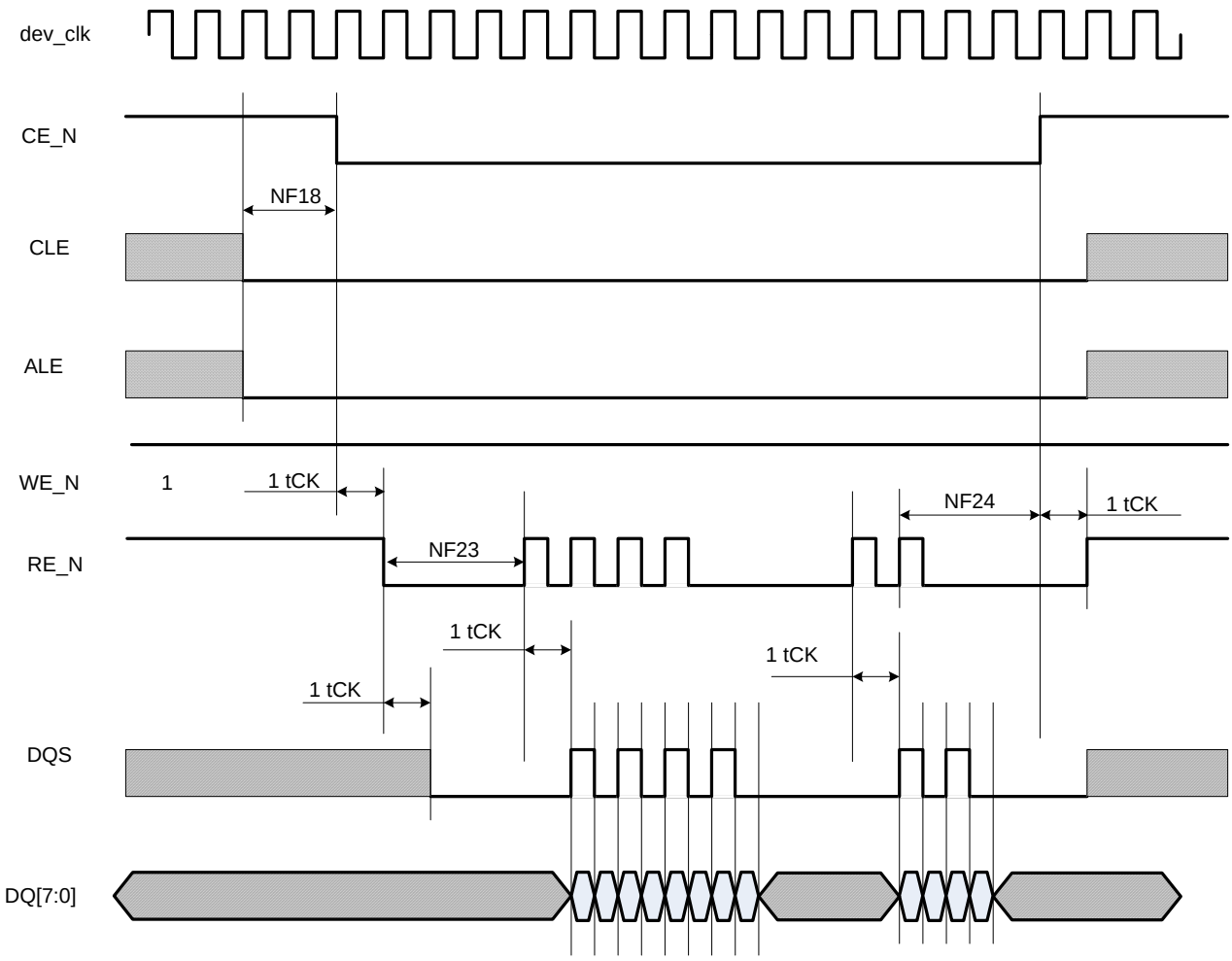


Figure 35. Samsung Toggle Mode Data Read Timing

Table 52. Samsung Toggle Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	CE# access time	tCE	CE_DELAY*tCK	—	ns
NF19	CE# hold time	tCH	0.5 *tCK	—	ns
NF20	Command/address DQ setup time	tCAS	0.5*tCK	—	ns
NF21	Command/address DQ hold time	tCAH	0.5*tCK	—	ns
NF22	clock period	tCK	7.5	--	ns

Table 52. Samsung Toggle Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF23	preamble delay	tPRE	(PRE_DELAY+1)*tCK	—	ns
NF24	postamble delay	tPOST	POST_DELAY*tCK	—	ns
NF25	CLE and ALE setup time	tCALS	0.5*tCK	—	ns
NF26	CLE and ALE hold time	tCALH	0.5*tCK	—	ns

1 GPMI's Sync Mode output timing could be controlled by module's internal registers, say HW_GPMI_TIMING2_CE_DELAY, HW_GPMI_TIMING_PREAMBLE_DELAY, and HW_GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers' setting. In the above table, we use CE_DELAY/PRE_DELAY/POST_DELAY to represent each of these settings.

4.11 External Peripheral Interface Parameters

The following subsections provide information on external peripheral interfaces.

4.11.1 AUDMUX Timing Parameters

The AUDMUX provides a programmable interconnect logic for voice, audio, and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is governed by the SSI module. For more information, see the respective SSI electrical specifications found within this document.

4.11.2 ECSPI Timing Parameters

This section describes the timing parameters of the ECSPI blocks. The ECSPI have separate timing parameters for master and slave modes.

4.11.2.1 ECSPI Master Mode Timing

Figure 36 depicts the timing of ECSPI in master mode. Table 53 lists the ECSPI master mode timing characteristics.

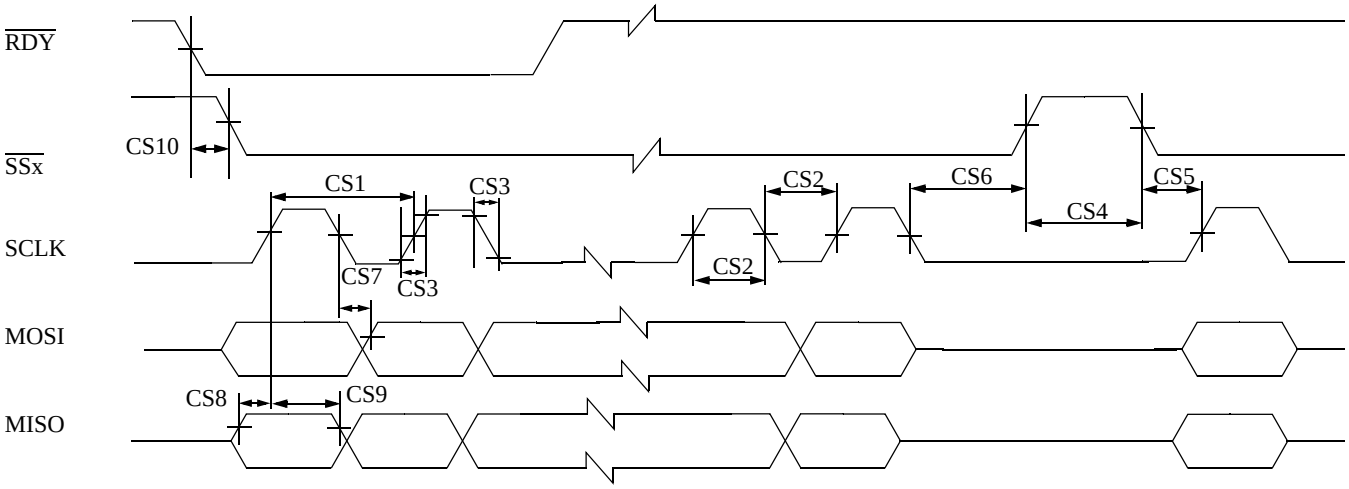


Figure 36. ECSPI Master Mode Timing Diagram

Table 53. ECSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time–Read SCLK Cycle Time–Write	t_{clk}	30 15	—	ns
CS2	SCLK High or Low Time–Read SCLK High or Low Time–Write	t_{SW}	14 7	—	ns
CS3	SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	SSx pulse width	t_{CSLH}	Half SCLK period	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-0.5	2.5	ns
CS8	MISO Setup Time	t_{Smiso}	8.5	—	ns
CS9	MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	RDY to SSx Time[2]	t_{SDRY}	5	—	ns

1 See Section 4.7, "I/O AC Parameters" for specific I/O AC parameters.

2 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other ECSPI signals.

4.11.2.2 ECSPI Slave Mode Timing

Figure 37 depicts the timing of ECSPI in slave mode. Table 54 lists the ECSPI slave mode timing characteristics.

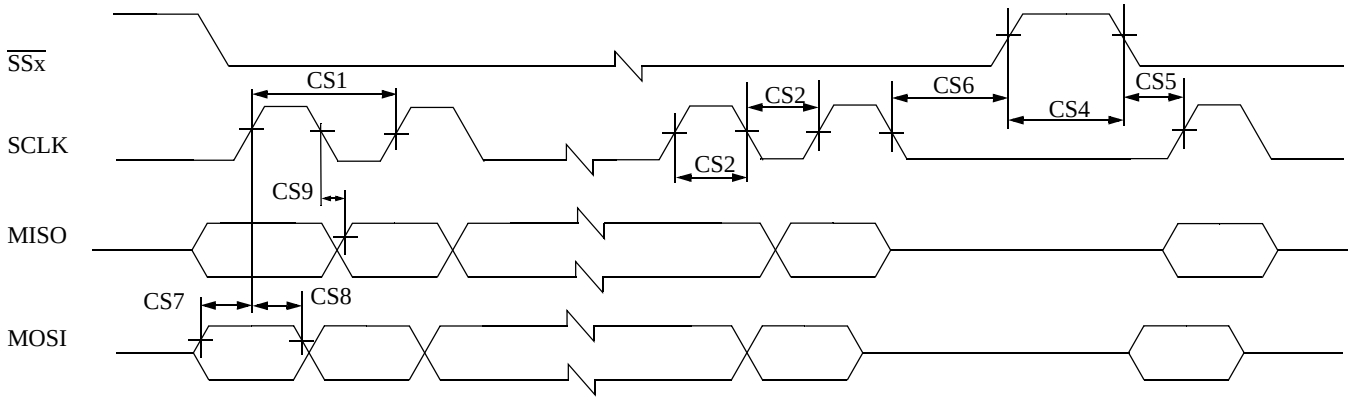


Figure 37. ECSPI Slave Mode Timing Diagram

Table 54. ECSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time–Read SCLK Cycle Time–Write	t_{clk}	15 40	—	ns
CS2	SCLK High or Low Time–Read SCLK High or Low Time–Write	t_{SW}	7 20	—	ns
CS4	SSx pulse width	t_{CSLH}	Half SCLK period	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	4	17	ns

4.11.3 Enhanced Serial Audio Interface (ESAI) Timing Parameters

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 55 shows the interface timing values. The number field in the table refers to timing signals found in Figure 38 and Figure 39.

Table 55. Enhanced Serial Audio Interface (ESAI) Timing

No.	Characteristics[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
62	Clock cycle[4]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period: • For internal clock • For external clock	 — —	 $2 \times T_C - 9.0$ $2 \times T_C$	 6 15	 — —	 — —	ns
64	Clock low period: • For internal clock • For external clock	 — —	 $2 \times T_C - 9.0$ $2 \times T_C$	 6 15	 — —	 — —	ns
65	SCKR rising edge to FSR out (bl) high	— —	— —	— —	17.0 7.0	x ck i ck a	ns
66	SCKR rising edge to FSR out (bl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
67	SCKR rising edge to FSR out (wr) high[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	SCKR rising edge to FSR out (wr) low[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	SCKR rising edge to FSR out (wl) high	— —	— —	— —	16.0 6.0	x ck i ck a	ns
70	SCKR rising edge to FSR out (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before SCKR (SCK in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after SCKR falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	FSR input (bl, wr) high before SCKR falling edge[5]	— —	— —	2.0 12.0	— —	x ck i ck a	ns
74	FSR input (wl) high before SCKR falling edge	— —	— —	2.0 12.0	— —	x ck i ck a	ns
75	FSR input hold time after SCKR falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
78	SCKT rising edge to FST out (bl) high	— —	— —	— —	18.0 8.0	x ck i ck	ns
79	SCKT rising edge to FST out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
80	SCKT rising edge to FST out (wr) high[5]	— —	— —	— —	20.0 10.0	x ck i ck	ns

Table 55. Enhanced Serial Audio Interface (ESAI) Timing (continued)

No.	Characteristics[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
81	SCKT rising edge to FST out (wr) low[5]	— —	— —	— —	22.0 12.0	x ck i ck	ns
82	SCKT rising edge to FST out (wl) high	— —	— —	— —	19.0 9.0	x ck i ck	ns
83	SCKT rising edge to FST out (wl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
84	SCKT rising edge to data out enable from high impedance	— —	— —	— —	22.0 17.0	x ck i ck	ns
86	SCKT rising edge to data out valid	— —	— —	— —	18.0 13.0	x ck i ck	ns
87	SCKT rising edge to data out high impedance [67]	— —	— —	— —	21.0 16.0	x ck i ck	ns
89	FST input (bl, wr) setup time before SCKT falling edge[5]	— —	— —	2.0 18.0	— —	x ck i ck	ns
90	FST input (wl) setup time before SCKT falling edge	— —	— —	2.0 18.0	— —	x ck i ck	ns
91	FST input hold time after SCKT falling edge	— —	— —	4.0 5.0	— —	x ck i ck	ns
95	HCKR/HCKT clock cycle	—	$2 \times T_C$	15	—	—	ns
96	HCKT input rising edge to SCKT output	—	—	—	18.0	—	ns
97	HCKR input rising edge to SCKR output	—	—	—	18.0	—	ns

1 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that SCKT and SCKR are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that SCKT and SCKR are the same clock)

2 bl = bit length
wl = word length
wr = word length relative

3 SCKT(SCKT pin) = transmit clock
SCKR(SCKR pin) = receive clock
FST(FST pin) = transmit frame sync
FSR(FSR pin) = receive frame sync
HCKT(HCKT pin) = transmit high frequency clock
HCKR(HCKR pin) = receive high frequency clock

4 For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

5 The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.

6 Periodically sampled and not 100% tested.

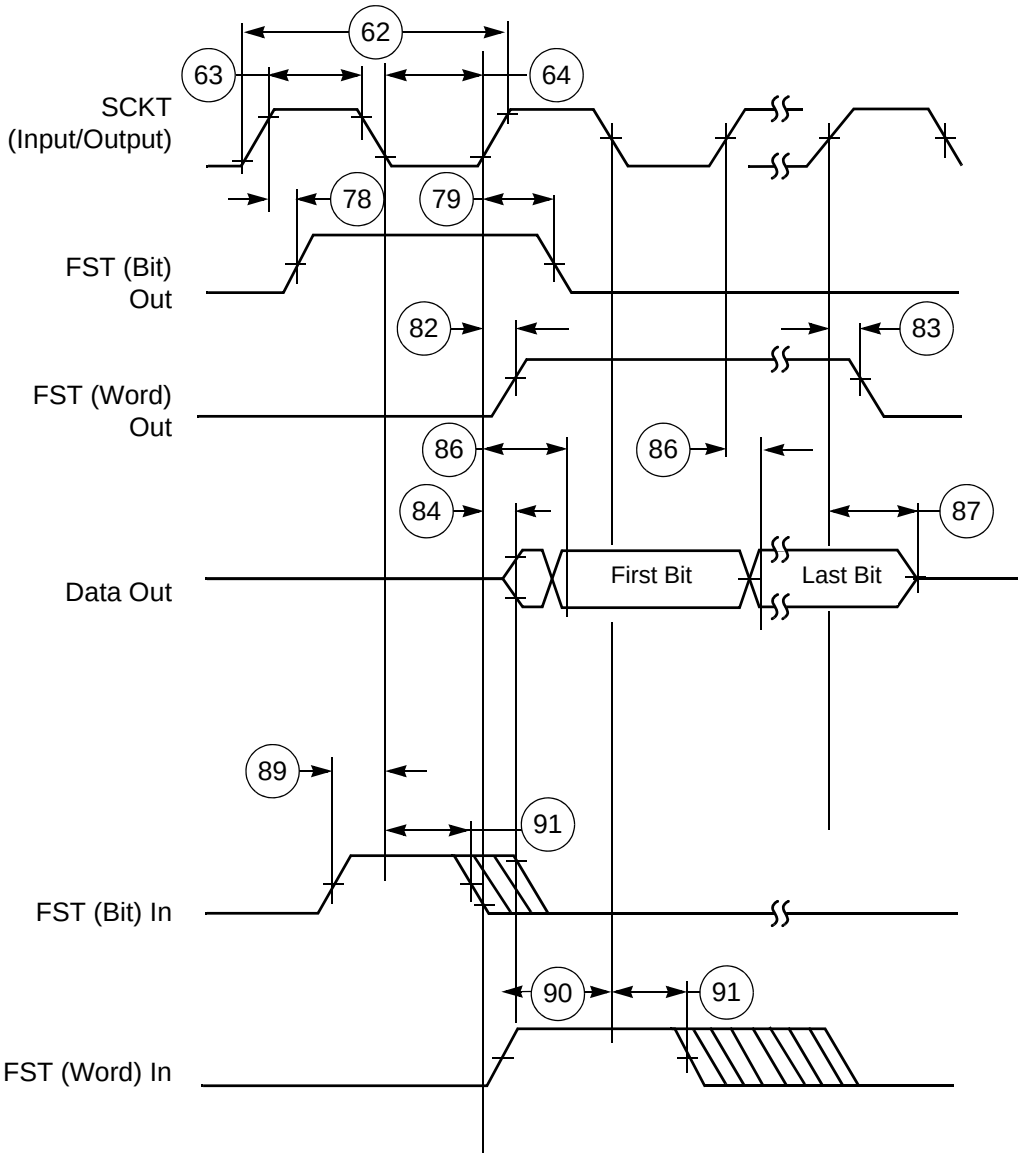


Figure 38. ESAI Transmitter Timing

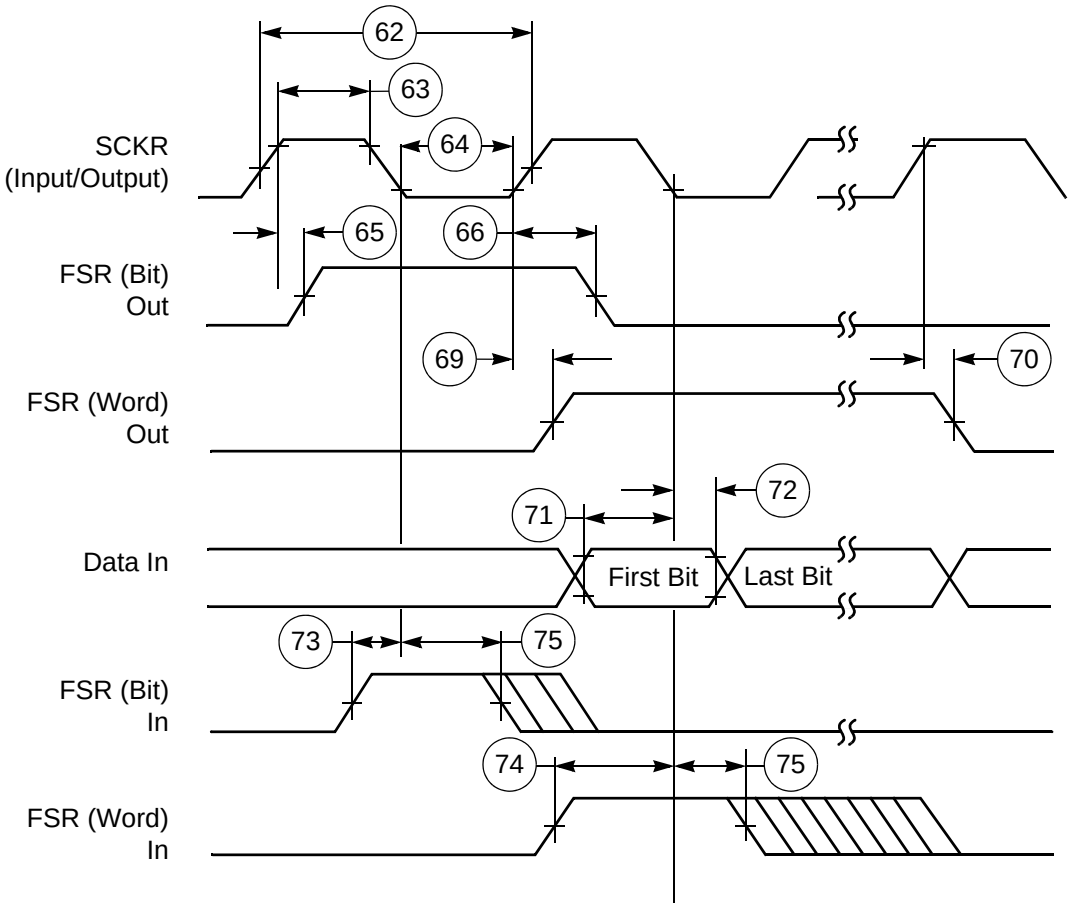


Figure 39. ESAI Receiver Timing

4.11.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4 (Dual Date Rate) timing.

4.11.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 40 depicts the timing of SD/eMMC4.3, and Table 56 lists the SD/eMMC4.3 timing characteristics.

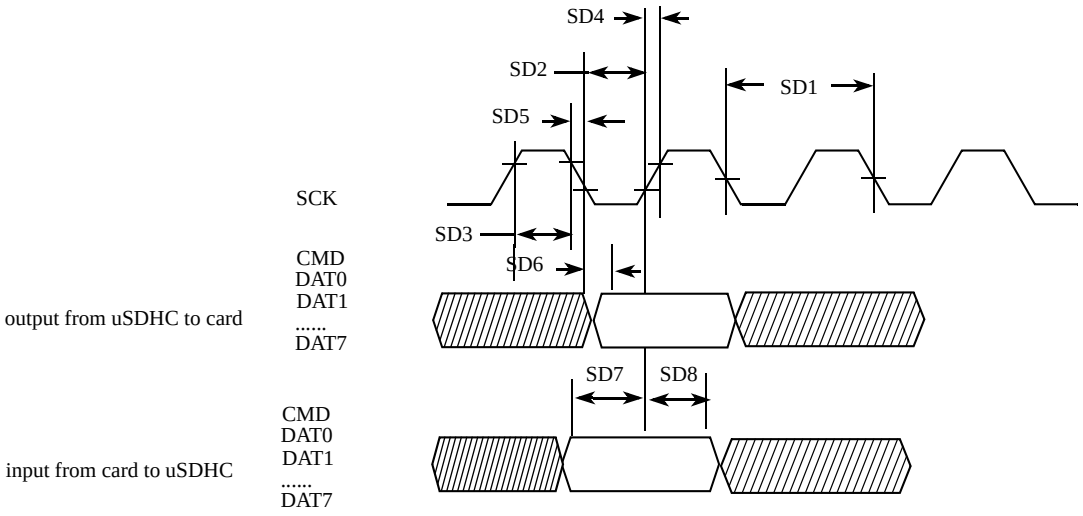


Figure 40. SD/eMMC4.3 Timing

Table 56. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs CMD, DAT (Reference to CLK)					
SD6	eSDHC Output Delay	t_{OD}	–5	2	ns

Table 56. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
eSDHC Input/Card Outputs CMD, DAT (Reference to CLK)					
SD7	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	eSDHC Input Hold Time[4]	t_{IH}	5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In high-speed mode, clock frequency can be any value between 0—50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In high-speed mode, clock frequency can be any value between 0—52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.11.4.2 eMMC4.4 (Dual Data Rate) eSDHCv3 AC Timing

Figure 41 depicts the timing of eMMC4.4. Table 57 lists the eMMC4.4 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

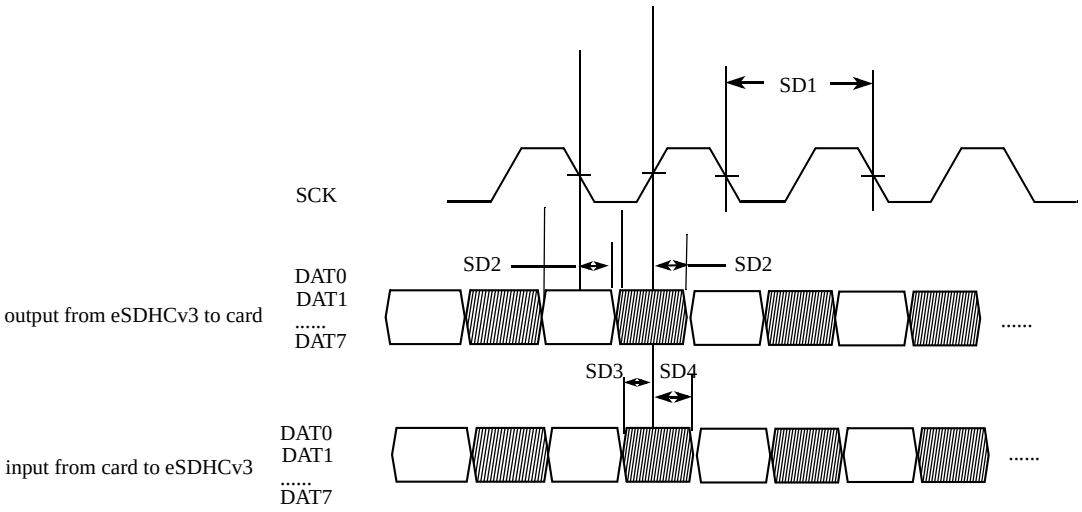


Figure 41. eMMC4.4 Timing

Table 57. eMMC4.4 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (EMMC4.4 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs CMD, DAT (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	–5	5	ns

Table 57. eMMC4.4 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Input / Card Outputs CMD, DAT (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	2.5	—	ns

4.11.4.3 SDR50/SDR104 AC Timing

Figure 42 depicts the timing of SDR50/SDR104, and Table 56 lists the SDR50/SDR104 timing characteristics.

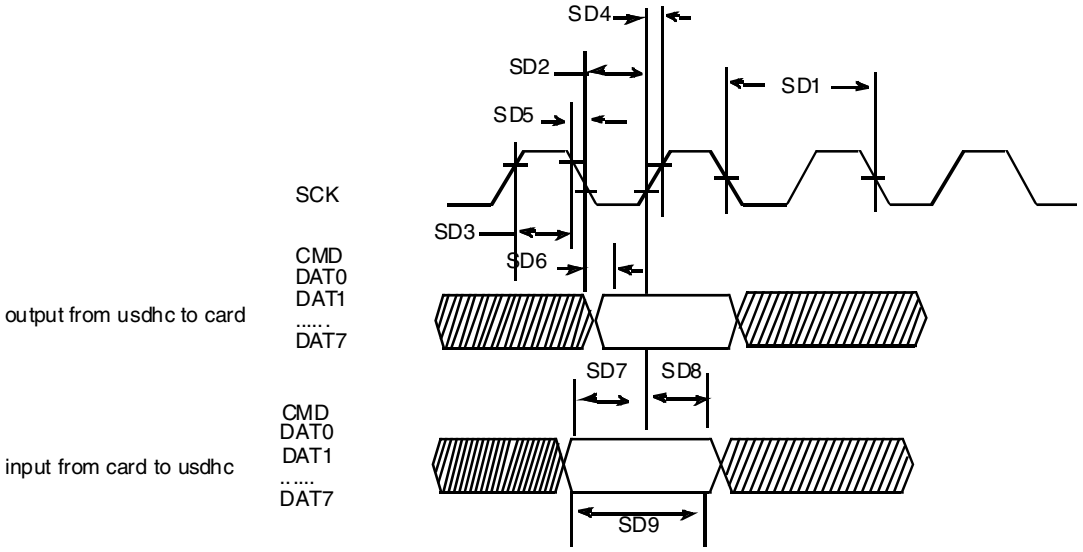


Figure 42. SDR50/SDR104 Timing

Table 58. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD5	Clock frequency	t_{CLK}	4.8	—	ns
SD6	Clock Low Time	$0.3*t_{CLK}$	$0.7*t_{CLK}$	—	ns
SD7	Clock High Time	$0.3*t_{CLK}$	$0.7*t_{CLK}$	—	ns
SD8	Clock Rise Time	t_{CR}	—	$0.2*t_{CLK}$	ns
SD9	Clock Fall Time	t_{CF}	—	$0.2*t_{CLK}$	ns
usdhc Output/Card Inputs CMD, DAT in SDR50 (Reference to CLK)					
SD10	uSDHC Output Delay	t_{OD}	–3	1	ns

Table 58. SDR50/SDR104 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
usdhc Output/Card Inputs CMD, DAT in SDR104 (Reference to CLK)					
SD6	uSDHC Output Delay	t_{OD}	–1	0.8	ns
usdhc Input/Card Outputs CMD, DAT in SDR50(Reference to CLK)					
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
usdhc Input/Card Outputs CMD, DAT in SDR104(Reference to CLK)[1]					
SD9	card output data window	t_{ODW}	$0.5*t_{CLK}$	—	ns

[1]Data window in SDR100 mode is variable.

4.11.5 Ethernet Controller (ENET) AC Electrical Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

4.11.5.1 MII Signal Switching Specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

Table 59. MII Signal Switching Specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	[O:] RXCLK pulse width high	35%	65%	RXCLK period
MII2	[O:] RXCLK pulse width low	35%	65%	RXCLK period
MII3	[O:] RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	[O:] RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	[O:] TXCLK frequency	—	25	MHz
MII5	[O:] TXCLK pulse width high	35%	65%	TXCLK period
MII6	[O:] TXCLK pulse width low	35%	65%	TXCLK period
MII7	[O:] TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	[O:] TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

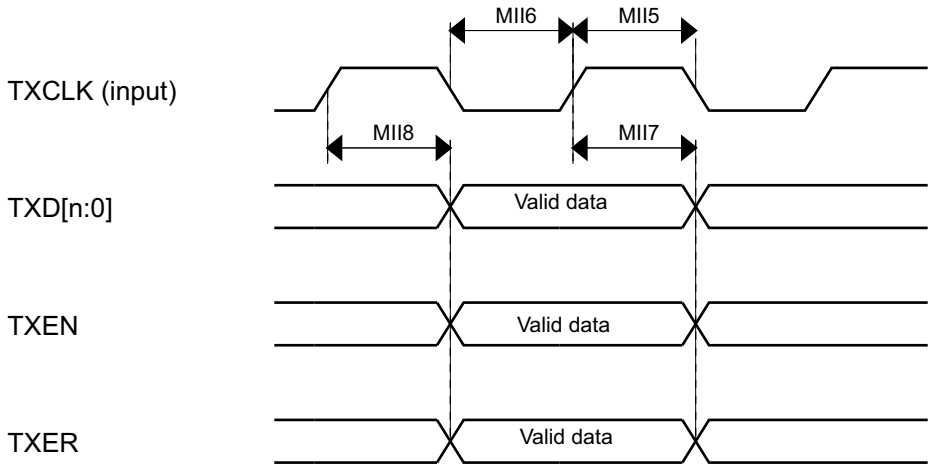


Figure 43. MII Transmit Signal Timing Diagram

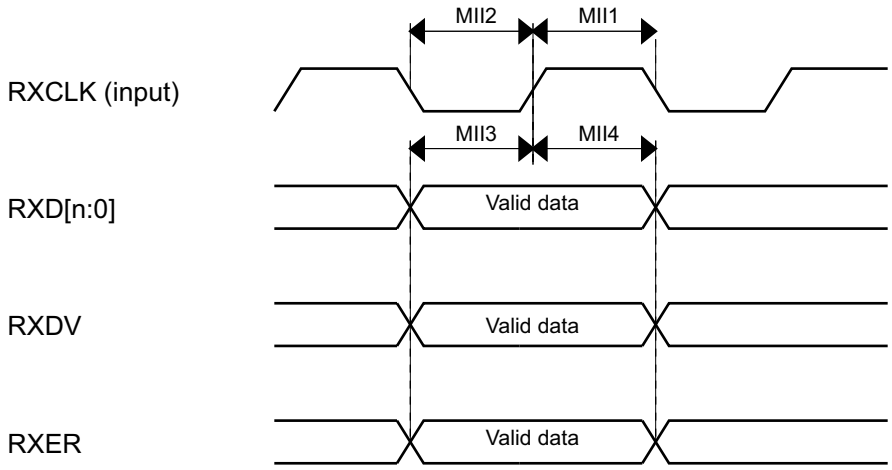


Figure 44. MII Receive Signal Timing Diagram

4.11.5.2 RMII Signal Switching Specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

Table 60. RMII Signal Switching Specifications

Symbol	Description	Min.	Max.	Unit
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
RMII1	[O:] RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2	[O:] RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	[O:] RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	[O:] RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
RMII7	[O:] RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns
RMII8	[O:] RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

4.11.5.3 RGMII Signal Switching Specifications

The following timing specs meet the requirements for RGMII style interfaces for a range of transceiver devices.

Table 61. RGMII Signal Switching Specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
Tcyc	Clock cycle duration	7.2	8.0	8.8	ns	1
TskewT	[O:] Data to clock output skew at transmitter	-500	0	500	ps	2
TskewR	[O:] Data to clock input skew at receiver	1	1.8	2.6	ps	2
TsetupT	[O:] Data to clock output setup (at transmitter with integrated delay)	1.2	2.0	—	ns	
TholdT	[O:] Data to clock output hold (at transmitter with integrated delay)	1.2	2.0	—	ns	
TsetupR	[O:] Data to clock input setup (at receiver with integrated delay)	1.0	2.0	—	ns	
TholdR	[O:] Data to clock input hold (at receiver with integrated delay)	1.0	2.0	—	ns	
Duty_G	[O:] Duty cycle for Gigabit	45	50	55	%	3
Duty_T	[O:] Duty cycle for 10/100T	40	50	60	%	3
Tr/Tf	[O:] Rise/fall time (20–80%)	—	—	0.75	ns	

1 For 10 Mbps and 100 Mbps, Tcyc will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

2 For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.

3 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

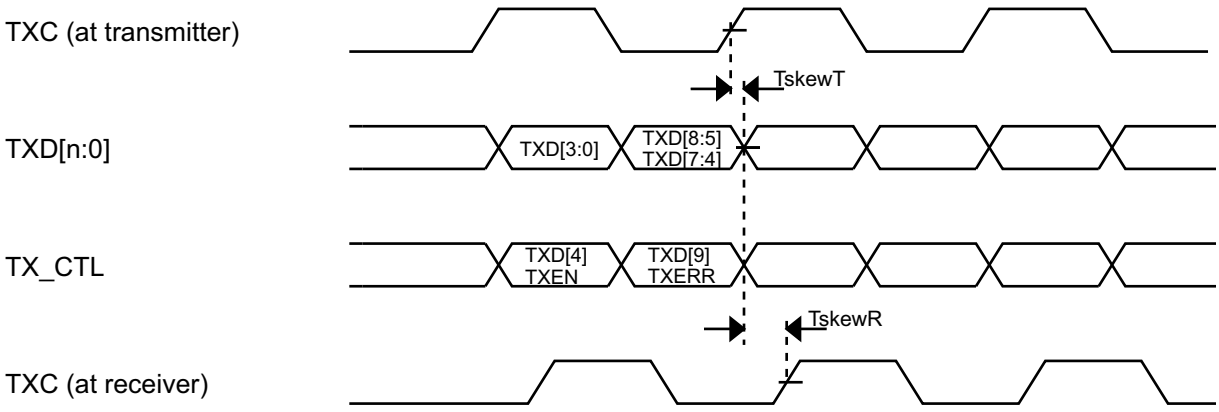


Figure 45. RGMII Transmit Signal Timing Diagram Original

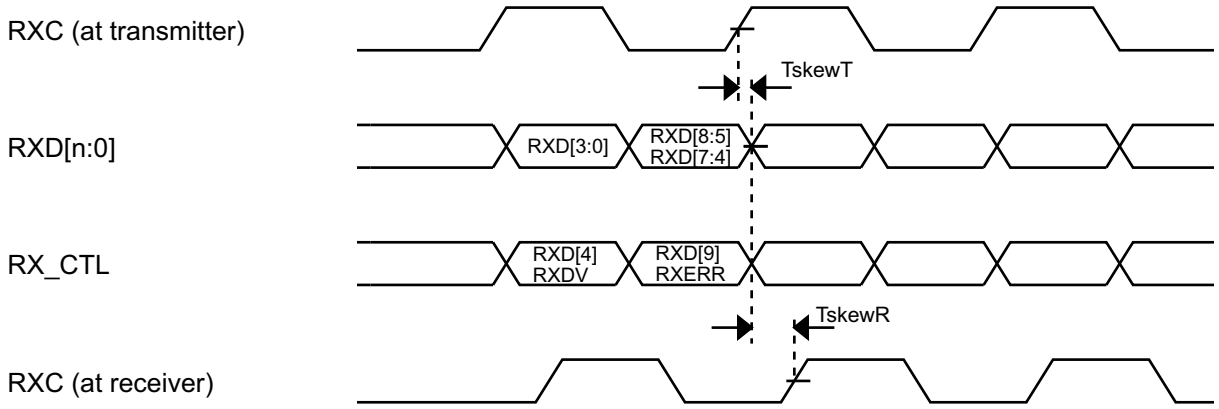


Figure 46. RGMII Receive Signal Timing Diagram Original

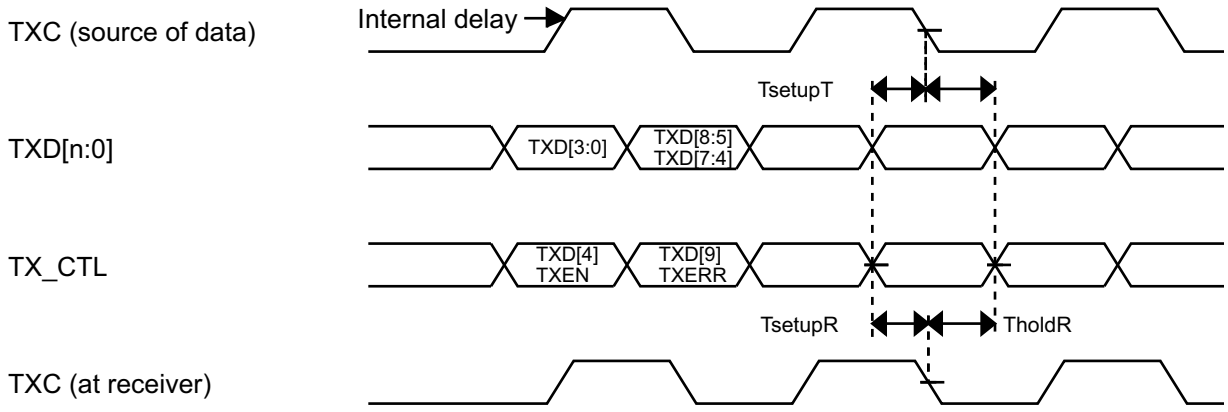


Figure 47. RGMII Transmit Signal Timing Diagram with Internal Delay

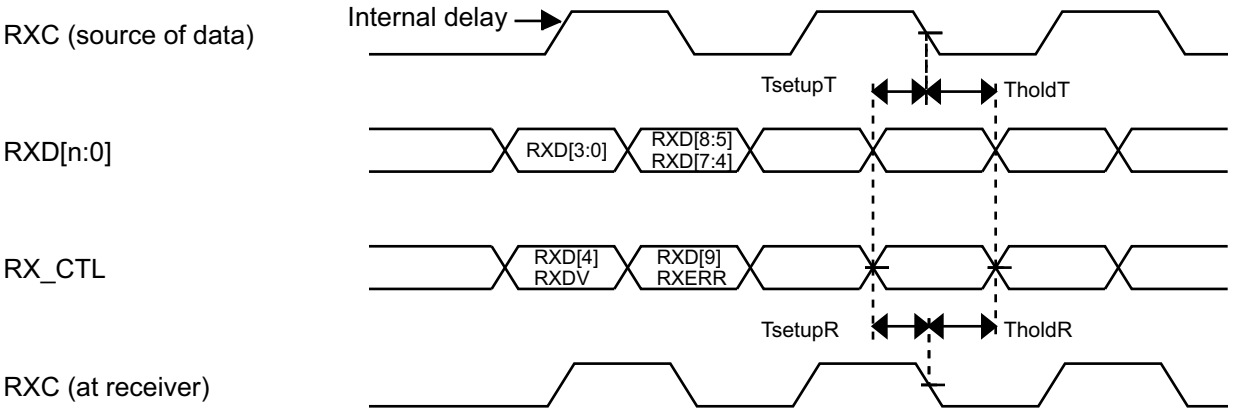


Figure 48. RGMII Receive Signal Timing Diagram with Internal Delay

4.11.6 Flexible Controller Area Network (FLEXCAN) AC Electrical Specifications

The electrical characteristics are related to the CAN transceiver (which is external to the processor), such as MC33902 from Freescale.The processor has two CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the i.MX 6Dual/6Quad reference manual to see which pins expose Tx and Rx pins; these ports are named TXCAN and RXCAN, respectively.

4.11.7 HDMI Module Timing Parameters

4.11.7.1 Latencies and Timing Information

Power-up time (time between TX_PWRON assertion and TX_READY assertion) for the HDMI 3D Tx PHY while operating with the slowest input reference clock supported (13.5 MHz) is 3.35 ms.

Power-up time for the HDMI 3D Tx PHY while operating with the fastest input reference clock supported (340 MHz) is 133MHz.

4.11.7.2 Electrical Characteristics

The table below provides electrical characteristics for the HDMI 3D Tx PHY. The following three figures illustrate various definitions and measurement conditions specified in the table below.

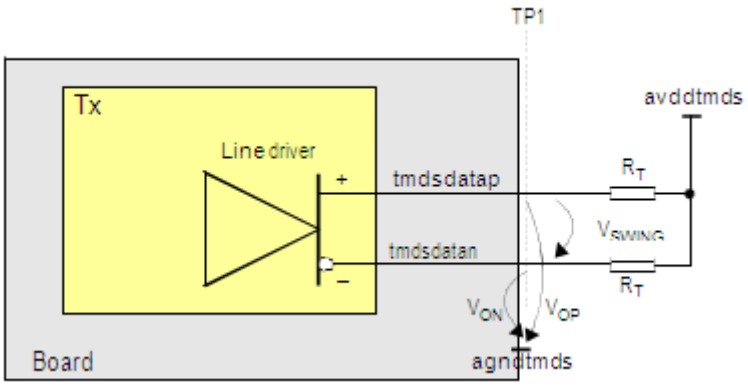


Figure 49. Driver Measuring Conditions

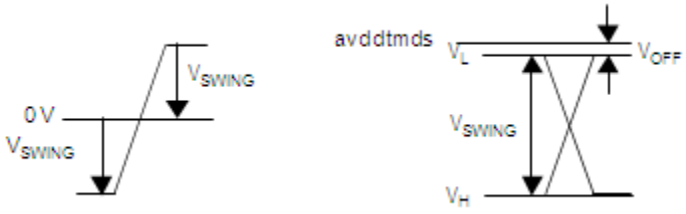


Figure 50. Driver Definitions

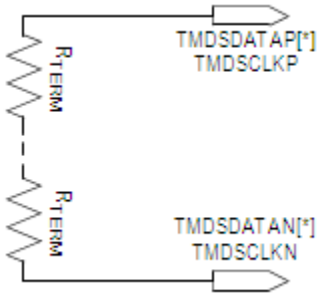


Figure 51. Source Termination

Table 62. Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Operating conditions for HDMI						
avddtmds	Termination supply voltage	-	3.15	3.3	3.45	V
R_T	Termination resistance	-	45	50	55	Ω
TMDS drivers DC specifications						
V_{OFF}	Single-ended standby voltage	RT = 50 Ω For measurement conditions and definitions, see the first two figures above. Compliance point TP1 as defined in the HDMI specification, version 1.3a, section 4.2.4.	avddtmds ± 10 mV			mV
V_{SWING}	Single-ended output swing voltage		400	-	600	mV
V_H	Single-ended output high voltage For definition, see the second figure above	If attached sink supports TMDSCLK < or = 165 MHz	avddtmds ± 10 mV			mV
		If attached sink supports TMDSCLK > 165 MHz	avddtmds – 200 mV	-	avddtmds + 10 mV	mV
V_L	Single-ended output low voltage For definition, see the second figure above	If attached sink supports TMDSCLK < or = 165 MHz	avddtmds – 600 mV	-	avddtmds – 400mV	mV
		If attached sink supports TMDSCLK > 165 MHz	avddtmds – 700 mV	-	avddtmds – 400 mV	mV
R_{TERM}	Differential source termination load (inside HDMI 3D Tx PHY) Although the HDMI 3D Tx PHY includes differential source termination, the user-defined value is set for each single line (for illustration, see the third figure above). **Note:** R_{TERM} can also be configured to be open and not present on TMDS channels.	-	50	-	200	Ω

Table 62. Electrical Characteristics (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Hot plug detect specifications						
HPD^{VH}	Hot plug detect high range	-	2.0	-	5.3	V
$VHPD_{VL}$	Hot plug detect low range	-	0	-	0.8	V
HPD_{Z}	Hot plug detect input impedance	-	10	-	-	kΩ
HPD_{t}	Hot plug detect time delay	-	-	-	100	µs

4.11.8 Switching Characteristics

Table 4-63 describes switching characteristics for the HDMI 3D Tx PHY. Figure 52 to Figure 60 illustrate various parameters specified in table.

NOTE

All dynamic parameters related to the TMDS line drivers' performance imply the use of assembly guidelines.

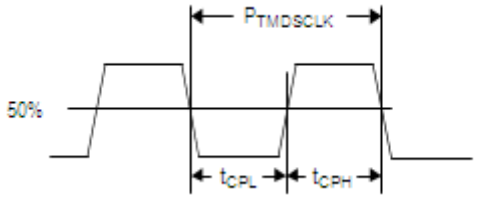


Figure 52. TMDS Clock Signal Definitions

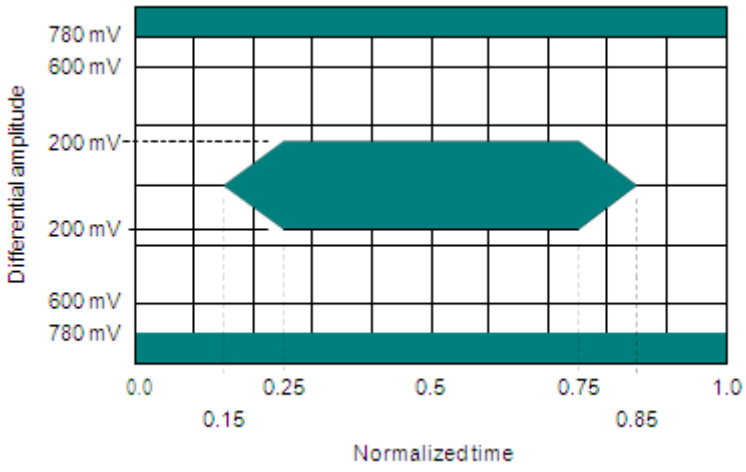


Figure 53. Eye Diagram Mask Definition for HDMI Driver Signal Specification at TP1

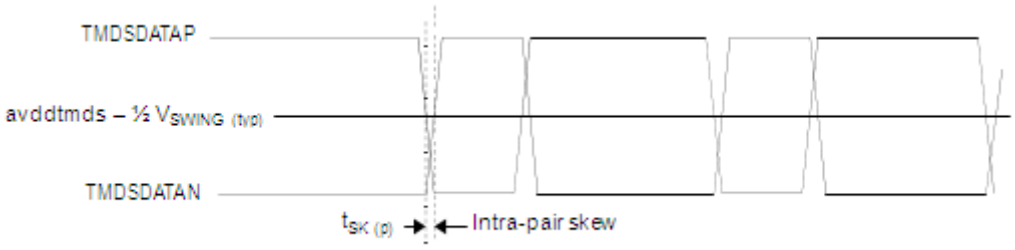


Figure 54. Intra-Pair Skew Definition

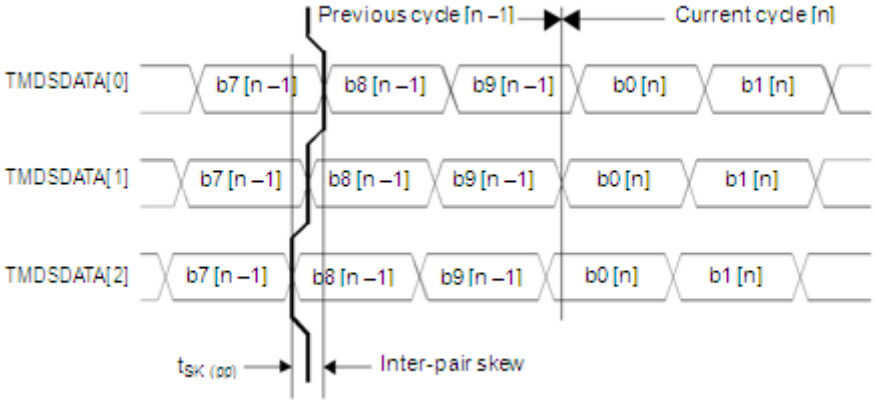


Figure 55. Inter-Pair Skew Definition

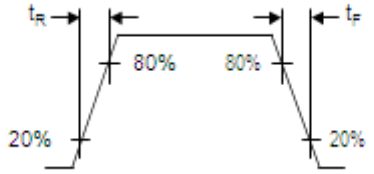


Figure 56. TMDS Output Signals Rise and Fall Time Definition

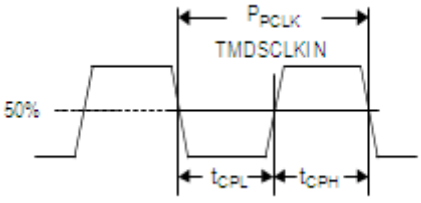


Figure 57. TMDSCLKIN/PCLK Signal Definitions

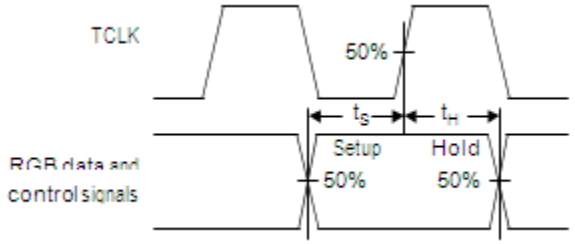


Figure 58. Digital Interface Input Signals Timing Definition

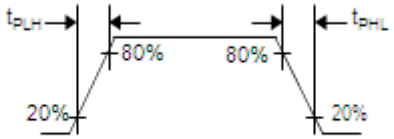


Figure 59. Digital Interface Switching Time Definition

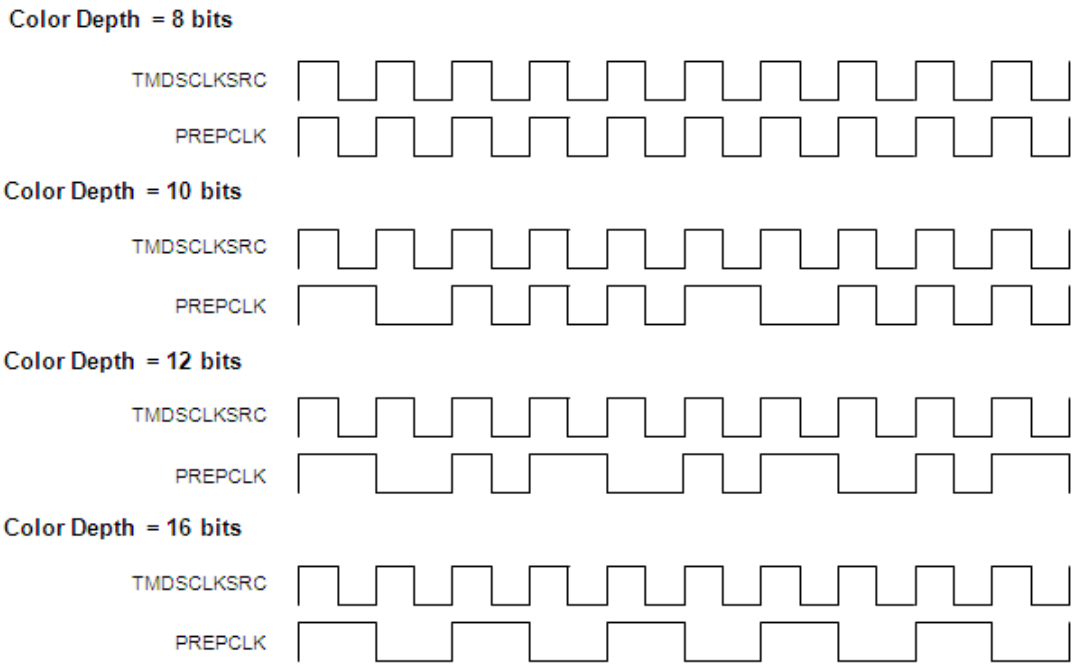


Figure 60. PREPCLK Frequencies Based on Color Depth

Table 4-63. Switching Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
TMDS Drivers Specifications						

Table 4-63. Switching Characteristics (continued)

—	Maximum serial data rate	—	—	—	3.4	Gbps
$F_{TMDSCLK}$	TMDSCLK frequency	On TMDSCLKP/N outputs	25	—	340	MHz
$P_{TMDSCLK}$	TMDSCLK period	RL = 50 Ω See Figure 52.	2.94	—	40	ns
t_{CDC}	TMDSCLK duty cycle	$t_{CDC} = t_{CPH} / P_{TMDSCLK}$ RL = 50 Ω See Figure 52.	40	50	60	%
t_{CPH}	TMDSCLK high time	RL = 50 Ω See Figure 52.	4	5	6	UI
t_{CPL}	TMDSCLK low time	RL = 50 Ω See Figure 52.	4	5	6	UI
—	TMDSCLK jitter[1]	RL = 50 Ω	—	—	0.25	UI
$t_{SK(p)}$	Intra-pair (pulse) skew	RL = 50 Ω See Figure 54.	—	—	0.15	UI
$t_{SK(pp)}$	Inter-pair skew	RL = 50 Ω See Figure 55.	—	—	1	UI
t_R	Differential output signal rise time	20–80% RL = 50 Ω See Figure 56.	75	—	0.4 UI	ps
t_F	Differential output signal fall time	20–80% RL = 50 Ω See Figure 56.	75	—	0.4 UI	ps
—	Differential signal overshoot	Referred to 2x V_{SWING}	—	—	15	%
—	Differential signal undershoot	Referred to 2x V_{SWING}	—	—	25	%
Data and Control Interface Specifications						
F_{PCLK}	PCLK frequency	Pixel repetition	13.5	—	340	MHz
P_{PCLK}	PCLK period	Pixel repetition	2.94	—	74	ns
		No pixel repetition	2.94	—	39.7	
$t_{CDC, PCLK}$	PCLK duty cycle	$t_{CDC,PCLK} = t_{CPH,PCLK} / P_{PCLK}$ See Figure 57.	40	—	60	%
$J_{rms, PCLK}$	PCLK long-term RMS jitter	—	—	—	100	ps
$F_{TMDSCLKIN}$	TMDSCLKIN frequency	—	12.5	—	340	MHz
$P_{TMDSCLKIN}$	TMDSCLKIN period	—	2.94	—	80	ns
$t_{CDC, TMDSCLKIN}$	TMDSCLKIN duty cycle	$t_{CDC,TMDSCLKIN} = t_{CPH,TMDSCLKIN} / P_{TMDSCLKIN}$ See Figure 57.				
		Normal mode	45	—	55	%
		Wide Interface mode	42.5	—	52.5	%
$F_{TMDSCLKSRC}$	TMDSCLKSRC frequency	—	12.5	—	340	MHz

Table 4-63. Switching Characteristics (continued)

$P_{TMDSCLKSRC}$	TMDSCLKSRC period	—	2.94	—	80	ns
$t_{CDC, MDSCLKSRC}$	TMDSCLKSRC duty cycle	—	42.5	—	52.5	%
$F_{PREPCLK}$	PREPCLK frequency	F_{PCLK} * pixel repetition PREPCLK = TMDSCLKSRC / {1, 1.25, 1.5, 2} Specified frequency of PREPCLK corresponds to its average frequency. See Figure 60.	—	—	340	MHz
t_S	Data/control setup time	Data signals.	1.5	—	—	ns
t_H	Data/control hold time	See Figure 58.	0	—	—	ns
t_{LH}, t_{HL}	Digital signals rise/fall times	See Figure 59.	—	—	200	ps
$t_{Power-up}$[2]	HDMI 3D Tx PHY power-up time	From power-down to TX_READY assertion	—	—	3.35	ms
Scan Interface Specifications						
F_{SCAN}	Scan clock frequency	—	—	—	42.5	MHz
I2C Interface Specifications						
F_{SCL}	Standard mode Fast Mode	—	—	—	100 400	KHz
$t_{HD, STA, I2C}$	Hold time (repeated) START condition	Standard Fast	4.0 .6	—	—	µs
$t_{LOW, SCL}$	Low period of SCL clock	Standard Fast	4.7 1.3	—	—	µs
$t_{HIGH, SCL}$	HIGH period of SCL clock	Standard Fast	4.0 .6	—	—	µs
$t_{SU, STA, I2C}$	Setup time (repeated) START condition	Standard Fast	4.7 .6	—		µs
$t_{HD, DAT, I2C}$	Data hold time[3]	Standard Fast	0[4]	—	—[5]	µs
$t_{SU, DAT, I2C}$	Data setup time	Standard Fast	250 100[6]	—	—	µs
$t_{SU, STO, I2C}$	Setup time for STOP condition	Standard Fast	4.0 .6	—	—	µs
$t_{BUF, I2C}$	Bus free time between START and STOP conditions	Standard Fast	4.7 1.3	—	—	µs
$t_{VD, DAT}$	Data valid time	Standard Fast	—	—	3.45 .9	µs
$t_{VD, ACK}$	Data valid acknowledgement time	Standard[7] Fast[8]	—	—	3.45 .9	µs

1 Relative to ideal recovery clock, as specified in the HDMI specification, version 1.4a, section 4.2.3.

2 For information about latencies and associated timings, see Section 4.11.7.1, “Latencies and Timing Information.”

3 $t_{HD, DAT}$ is the data hold time measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

4 A device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

5 The maximum $t_{HD, DAT}$ can be 3.45 µs for Standard mode and 0.9 µs for Fast mode, but must be less than the maximum of $t_{VD, DAT}$ or $t_{VD, ACK}$ by a transition time. This maximum must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set up time before the clock is released.

6 A Fast mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the required $t_{SU, DAT}$ 250 ns must then be met. This situation will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, the device must output the next data bit to the SDA line tr(max) + $t_{SU, DAT}$ = 1,000 + 250 = 1,250 ns (according to the Standard mode I²C bus specification) before the SCL line is released. In addition, the acknowledge timing must meet this set up time.

7 $t_{VD, DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

8 $t_{VD, ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

4.11.9 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. Figure 61 depicts the timing of I²C module, and Table 64 lists the I²C module timing characteristics.

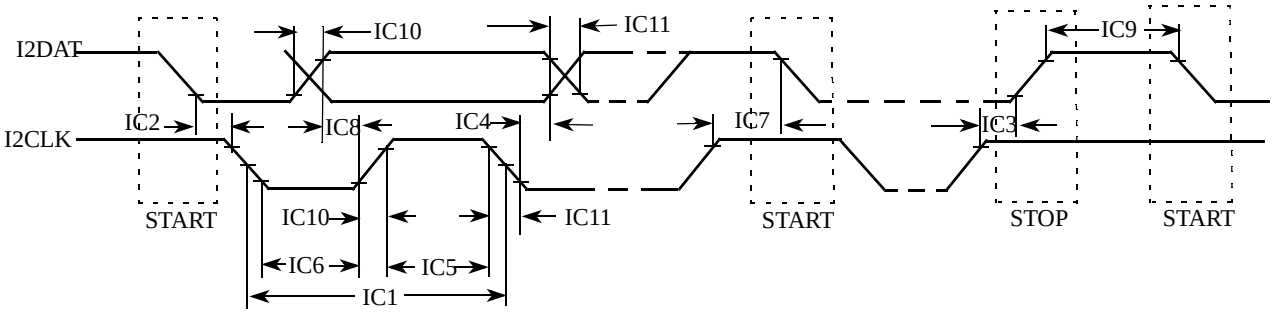


Figure 61. I²C Bus Timing

Table 64. I²C Module Timing Parameters

ID	Parameter	Standard Mode Supply Voltage = 1.65 V–1.95 V, 2.7 V–3.3 V		Fast Mode Supply Voltage = 2.7 V–3.3 V		Unit
		Min	Max	Min	Max	
IC1	I2CLK cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs

Table 64. I^2C Module Timing Parameters (continued)

ID	Parameter	Standard Mode Supply Voltage = 1.65 V–1.95 V, 2.7 V–3.3 V		Fast Mode Supply Voltage = 2.7 V–3.3 V		Unit
		Min	Max	Min	Max	
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal.

3 A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2CLK line is released.

4 C_b = total capacitance of one bus line in pF.

4.11.10 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, and other related functions.
- Synchronization and control capabilities, such as avoidance of tearing artifacts.

4.11.10.1 IPU Sensor Interface Signal Mapping

The IPU supports a number of sensor input formats. Table 65 defines the mapping of the Sensor Interface Pins used for various supported interface formats.

Table 65. Camera Input Signal Cross Reference, Format, and Bits Per Cycle

Signal Name[1]	RGB565 8 bits 2 cycles	RGB565[2] 8 bits 3 cycles	RGB666[3] 8 bits 3 cycles	RGB888 8 bits 3 cycles	YCbCr 8 bits 2 cycles	RGB565[4] 16 bits 2 cycles	YCbCr[5] 16 bits 1 cycle	YCbCr[6] 16 bits 1 cycle	YCbCr[7] 20 bits 1 cycle
CSIx_DAT0	—	—	—	—	—	—	—	0	C[0]
CSIx_DAT1	—	—	—	—	—	—	—	0	C[1]
CSIx_DAT2	—	—	—	—	—	—	—	C[0]	C[2]
CSIx_DAT3	—	—	—	—	—	—	—	C[1]	C[3]
CSIx_DAT4	—	—	—	—	—	B[0]	C[0]	C[2]	C[4]
CSIx_DAT5	—	—	—	—	—	B[1]	C[1]	C[3]	C[5]
CSIx_DAT6	—	—	—	—	—	B[2]	C[2]	C[4]	C[6]
CSIx_DAT7	—	—	—	—	—	B[3]	C[3]	C[5]	C[7]
CSIx_DAT8	—	—	—	—	—	B[4]	C[4]	C[6]	C[8]
CSIx_DAT9	—	—	—	—	—	G[0]	C[5]	C[7]	C[9]
CSIx_DAT10	—	—	—	—	—	G[1]	C[6]	0	Y[0]
CSIx_DAT11	—	—	—	—	—	G[2]	C[7]	0	Y[1]
CSIx_DAT12	B[0], G[3]	R[2],G[4],B[2]	R/G/B[4]	R/G/B[0]	Y/C[0]	G[3]	Y[0]	Y[0]	Y[2]
CSIx_DAT13	B[1], G[4]	R[3],G[5],B[3]	R/G/B[5]	R/G/B[1]	Y/C[1]	G[4]	Y[1]	Y[1]	Y[3]
CSIx_DAT14	B[2], G[5]	R[4],G[0],B[4]	R/G/B[0]	R/G/B[2]	Y/C[2]	G[5]	Y[2]	Y[2]	Y[4]
CSIx_DAT15	B[3], R[0]	R[0],G[1],B[0]	R/G/B[1]	R/G/B[3]	Y/C[3]	R[0]	Y[3]	Y[3]	Y[5]
CSIx_DAT16	B[4], R[1]	R[1],G[2],B[1]	R/G/B[2]	R/G/B[4]	Y/C[4]	R[1]	Y[4]	Y[4]	Y[6]
CSIx_DAT17	G[0], R[2]	R[2],G[3],B[2]	R/G/B[3]	R/G/B[5]	Y/C[5]	R[2]	Y[5]	Y[5]	Y[7]
CSIx_DAT18	G[1], R[3]	R[3],G[4],B[3]	R/G/B[4]	R/G/B[6]	Y/C[6]	R[3]	Y[6]	Y[6]	Y[8]
CSIx_DAT19	G[2], R[4]	R[4],G[5],B[4]	R/G/B[5]	R/G/B[7]	Y/C[7]	R[4]	Y[7]	Y[7]	Y[9]

1 CSIx stands for CSI1 or CSI2

2 The MSB bits are duplicated on LSB bits implementing color extension

3 The two MSB bits are duplicated on LSB bits implementing color extension

4 RGB 16 bits – supported in two ways: (1) As a “generic data” input – with no on-the-fly processing; (2) With on-the-fly processing, but only under some restrictions on the control protocol.

5 YCbCr 16 bits - supported as a “generic-data” input – with no on-the-fly processing.

6 YCbCr 16 bits - supported as a sub-case of the YCbCr, 20 bits, under the same conditions (BT.1120 protocol).

7 YCbCr, 20 bits, supported only within the BT.1120 protocol (syncs embedded within the data stream).

4.11.10.2 Sensor Interface Timings

There are three camera timing modes supported by the IPU.

4.11.10.2.1 BT.656 and BT.1120 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the SENSB_VSYNC and SENSB_HSYNC signals. The timing syntax is defined by the BT.656/BT.1120 standards.

This operation mode follows the recommendations of ITU BT.656/ ITU BT.1120 specifications. The only control signal used is SENSB_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering SENSB_VSYNC and SENSB_HSYNC signals for internal use. On BT.656 one component per cycle is received over the SENSB_DATA bus. On BT.1120 two components per cycle are received over the SENSB_DATA bus.

4.11.10.2.2 Gated Clock Mode

The SENSB_VSYNC, SENSB_HSYNC, and SENSB_PIX_CLK signals are used in this mode. See Figure 62.

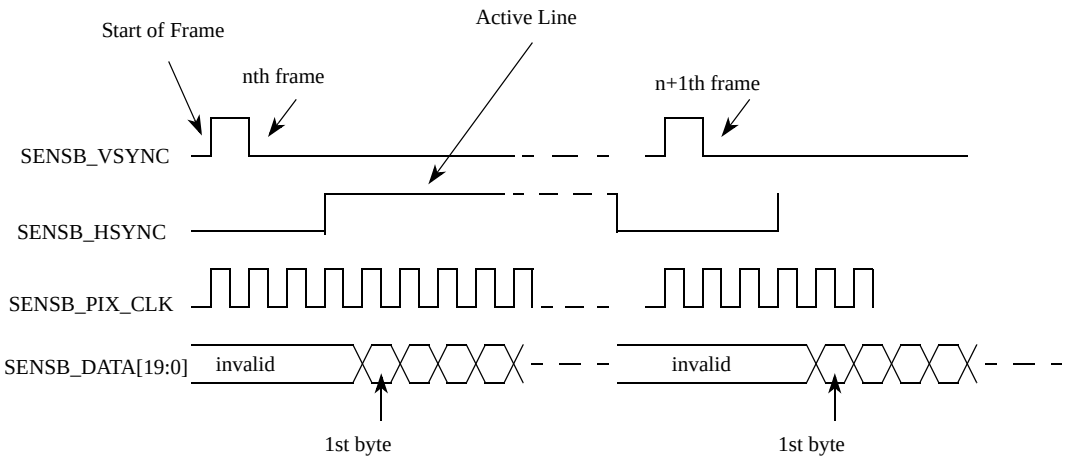


Figure 62. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on SENSB_VSYNC (all the timings correspond to straight polarity of the corresponding signals). Then SENSB_HSYNC goes to high and hold for the entire line. Pixel clock is valid as long as SENSB_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. SENSB_HSYNC goes to low at the end of line. Pixel clocks then become invalid and the CSI stops receiving data from the stream. For next line the SENSB_HSYNC timing repeats. For next frame the SENSB_VSYNC timing repeats.

4.11.10.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in Section 4.11.10.2.2, “Gated Clock Mode,”) except for the SENSB_HSYNC signal, which is not used (see Figure 63). All incoming pixel clocks are

valid and cause data to be latched into the input FIFO. The SENSB_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

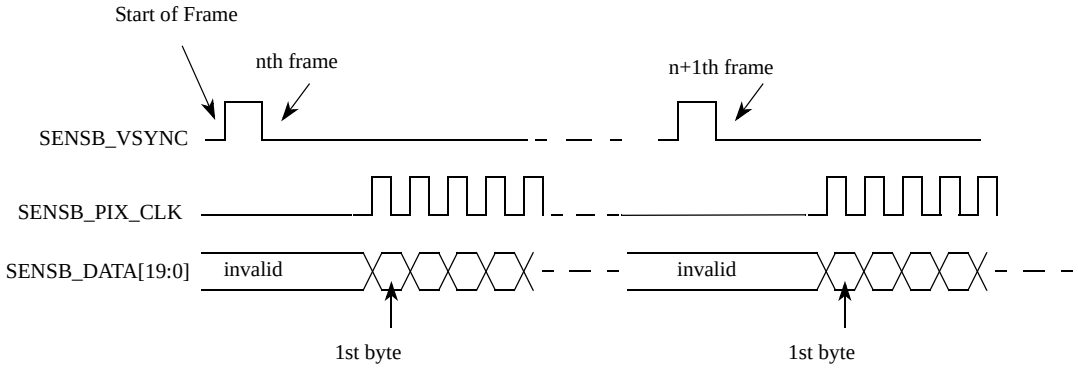


Figure 63. Non-Gated Clock Mode Timing Diagram

The timing described in Figure 63 is that of a typical sensor. Some other sensors may have a slightly different timing. The CSI can be programmed to support rising/falling-edge triggered SENSB_VSYNC; active-high/low SENSB_HSYNC; and rising/falling-edge triggered SENSB_PIX_CLK.

4.11.10.3 Electrical Characteristics

Figure 64 depicts the sensor interface timing. SENSB_MCLK signal described here is not generated by the IPU. Table 66 lists the sensor interface timing characteristics.

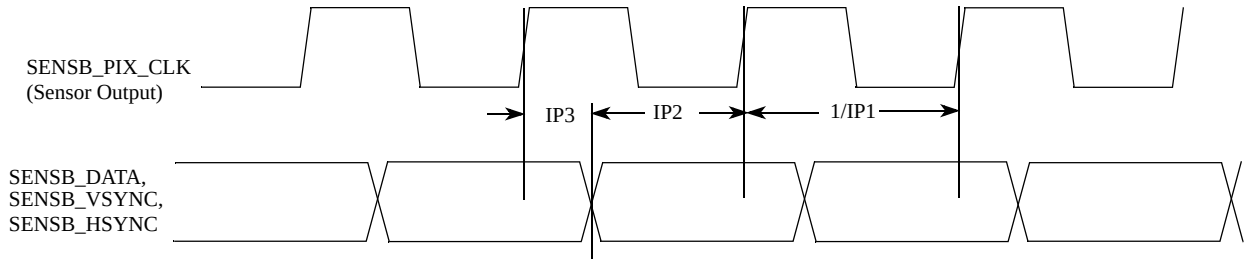


Figure 64. Sensor Interface Timing Diagram

Table 66. Sensor Interface Timing Characteristics

ID	Parameter	Symbol	Min	Max	Unit
IP1	Sensor output (pixel) clock frequency	Fpck	0.01	180	MHz
IP2	Data and control setup time	Tsu	2	—	ns
IP3	Data and control holdup time	Thd	1	—	ns

4.11.10.4 IPU Display Interface Signal Mapping

The IPU supports a number of display output video formats. Table 67 defines the mapping of the Display Interface Pins used during various supported video interface formats.

Table 67. Video Signal Cross-Reference

i.MX 6Dual/6Quad	LCD							Comment[1]
Port Name (x=0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						Smart
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[2]	16-bit YCrCb	20-bit YCrCb	Signal Name	
DISPx_DAT0	DAT[0]	B[0]	B[0]	B[0]	Y/C[0]	C[0]	C[0]	DAT[0]	The restrictions are as follows: • There are maximal three continuous groups of bits that could be independently mapped to the external bus. Groups should not be overlapped. • The bit order is expressed in each of the bit groups, for example, B[0] = least significant blue pixel bit
DISPx_DAT1	DAT[1]	B[1]	B[1]	B[1]	Y/C[1]	C[1]	C[1]	DAT[1]	
DISPx_DAT2	DAT[2]	B[2]	B[2]	B[2]	Y/C[2]	C[2]	C[2]	DAT[2]	
DISPx_DAT3	DAT[3]	B[3]	B[3]	B[3]	Y/C[3]	C[3]	C[3]	DAT[3]	
DISPx_DAT4	DAT[4]	B[4]	B[4]	B[4]	Y/C[4]	C[4]	C[4]	DAT[4]	
DISPx_DAT5	DAT[5]	G[0]	B[5]	B[5]	Y/C[5]	C[5]	C[5]	DAT[5]	
DISPx_DAT6	DAT[6]	G[1]	G[0]	B[6]	Y/C[6]	C[6]	C[6]	DAT[6]	
DISPx_DAT7	DAT[7]	G[2]	G[1]	B[7]	Y/C[7]	C[7]	C[7]	DAT[7]	
DISPx_DAT8	DAT[8]	G[3]	G[2]	G[0]	—	Y[0]	C[8]	DAT[8]	
DISPx_DAT9	DAT[9]	G[4]	G[3]	G[1]	—	Y[1]	C[9]	DAT[9]	
DISPx_DAT10	DAT[10]	G[5]	G[4]	G[2]	—	Y[2]	Y[0]	DAT[10]	
DISPx_DAT11	DAT[11]	R[0]	G[5]	G[3]	—	Y[3]	Y[1]	DAT[11]	
DISPx_DAT12	DAT[12]	R[1]	R[0]	G[4]	—	Y[4]	Y[2]	DAT[12]	
DISPx_DAT13	DAT[13]	R[2]	R[1]	G[5]	—	Y[5]	Y[3]	DAT[13]	
DISPx_DAT14	DAT[14]	R[3]	R[2]	G[6]	—	Y[6]	Y[4]	DAT[14]	
DISPx_DAT15	DAT[15]	R[4]	R[3]	G[7]	—	Y[7]	Y[5]	DAT[15]	
DISPx_DAT16	DAT[16]	—	R[4]	R[0]	—	—	Y[6]	—	
DISPx_DAT17	DAT[17]	—	R[5]	R[1]	—	—	Y[7]	—	
DISPx_DAT18	DAT[18]	—	—	R[2]	—	—	Y[8]	—	
DISPx_DAT19	DAT[19]	—	—	R[3]	—	—	Y[9]	—	
DISPx_DAT20	DAT[20]	—	—	R[4]	—	—	—	—	
DISPx_DAT21	DAT[21]	—	—	R[5]	—	—	—	—	

Table 67. Video Signal Cross-Reference (continued)

i.MX 6Dual/6Quad	LCD								Comment[1]
Port Name (x=0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						Smart	
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[2]	16-bit YCrCb	20-bit YCrCb	Signal Name	
DISPx_DAT22	DAT[22]	—	—	R[6]	—	—	—	—	—
DISPx_DAT23	DAT[23]	—	—	R[7]	—	—	—	—	—
DIx_DISP_CLK	PixCLK							—	—
DIx_PIN1	—							VSYNC_IN	May be required for anti-tearing
DIx_PIN2	HSYNC							—	—
DIx_PIN3	VSYNC							—	VSYNC out
DIx_PIN4	—							—	Additional frame/row synchronous signals with programmable timing
DIx_PIN5	—							—	
DIx_PIN6	—							—	
DIx_PIN7	—							—	
DIx_PIN8	—							—	
DIx_D0_CS	—							CS0	—
DIx_D1_CS	—							CS1	Alternate mode of PWM output for contrast or brightness control
DIx_PIN11	—							WR	—
DIx_PIN12	—							RD	—
DIx_PIN13	—							RS1	Register select signal
DIx_PIN14	—							RS2	Optional RS2
DIx_PIN15	DRDY/DV							DRDY	Data validation/blank, data enable
DIx_PIN16	—							—	Additional data synchronous signals with programmable features/timing
DIx_PIN17	Q							—	

1 Signal mapping (both data and control/synchronization) is flexible. The table provides examples.

2 This mode works in compliance with recommendation ITU-R BT.656. The timing reference signals (frame start, frame end, line start, and line end) are embedded in the 8-bit data bus. Only video data is supported, transmission of non-video related data during blanking intervals is not supported.

NOTE

Table 67 provides information for both the Disp0 and Disp1 ports. However, Disp1 port has reduced pinout depending on IOMUXC configuration and therefore may not support all the above configurations. See the IOMUXC table for details.

4.11.10.5 IPU Display Interface Timing

The IPU Display Interface supports two kinds of display accesses: synchronous and asynchronous. There are two groups of external interface pins to provide synchronous and asynchronous controls accordantly.

4.11.10.5.1 Synchronous Controls

The synchronous control changes its value as a function of a system or of an external clock. This control has a permanent period and a permanent wave form.

There are special physical outputs to provide synchronous controls:

- The ipp_disp_clk is a dedicated base synchronous signal that is used to generate a base display (component, pixel) clock for a display.
- The ipp_pin_1– ipp_pin_7 are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any else independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as, HSYNC/VSYCN) calculation. The internal event (local start point) is synchronized with internal DI_CLK. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half DI_CLK resolution. A full description of the counters system can be found in the IPU chapter of the i.MX 6Dual/6Quad reference manual.

4.11.10.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The ipp_d0_cs and ipp_d1_cs pins are dedicated to provide chip select signals to two displays.
- The ipp_pin_11– ipp_pin_17 are general purpose asynchronous pins, that can be used to provide WR. RD, RS or any other data oriented signal to display.

NOTE

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data in the bus, a new internal start (local start point) is generated. The signals generators calculate predefined UP and DOWN values to change pins states with half DI_CLK resolution.

4.11.10.6 Synchronous Interfaces to Standard Active Matrix TFT LCD Panels

4.11.10.6.1 IPU Display Operating Signals

The IPU uses four control signals and data to operate a standard synchronous interface:

- IPP_DISP_CLK—Clock to display
- HSYNC—Horizontal synchronization
- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on the base of an internally generated “local start point”. The synchronous display controls can be placed on time axis with DI’s offset, up and down parameters. The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point. The data bus of the synchronous interface is output direction only.

4.11.10.6.2 LCD Interface Functional Description

Figure 65 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure, signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DI_CLK internal DI clock is used for calculation of other controls.
- IPP_DISP_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, IPP_DISP_CLK runs continuously.
- HSYNC causes the panel to start a new line. (Usually IPP_PIN_2 is used as HSYNC.)
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse. (Usually IPP_PIN_3 is used as VSYNC.)
- DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.
(DRDY can be used either synchronous or asynchronous generic purpose pin as well.)

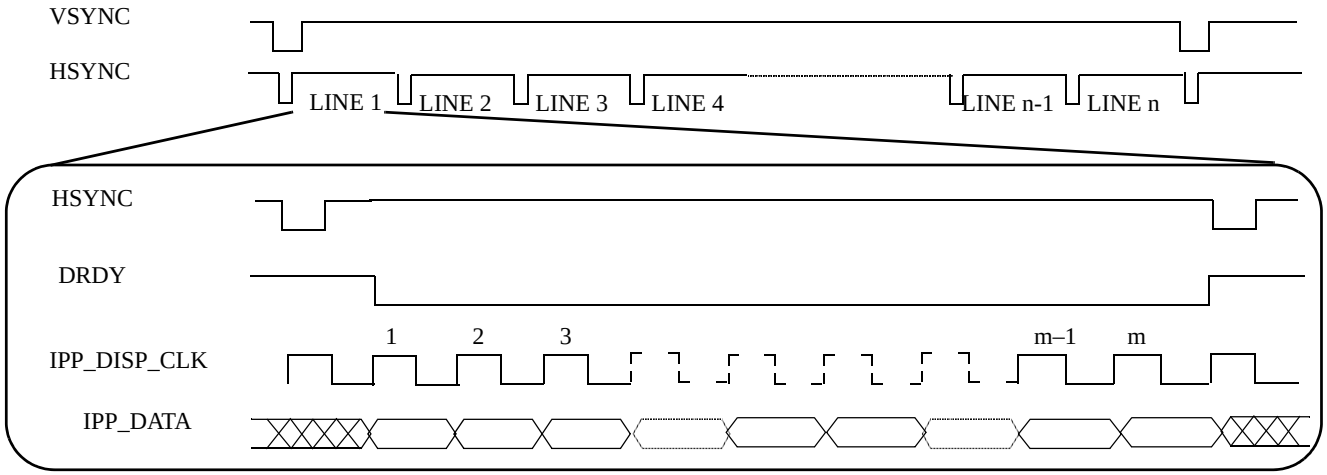


Figure 65. Interface Timing Diagram for TFT (Active Matrix) Panels

4.11.10.6.3 TFT Panel Sync Pulse Timing Diagrams

Figure 66 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All the parameters shown in the figure are programmable. All controls are started by corresponding internal events—local start points. The timing diagrams correspond to inverse polarity of the IPP_DISP_CLK signal and active-low polarity of the HSYNC, VSYNC, and DRDY signals.

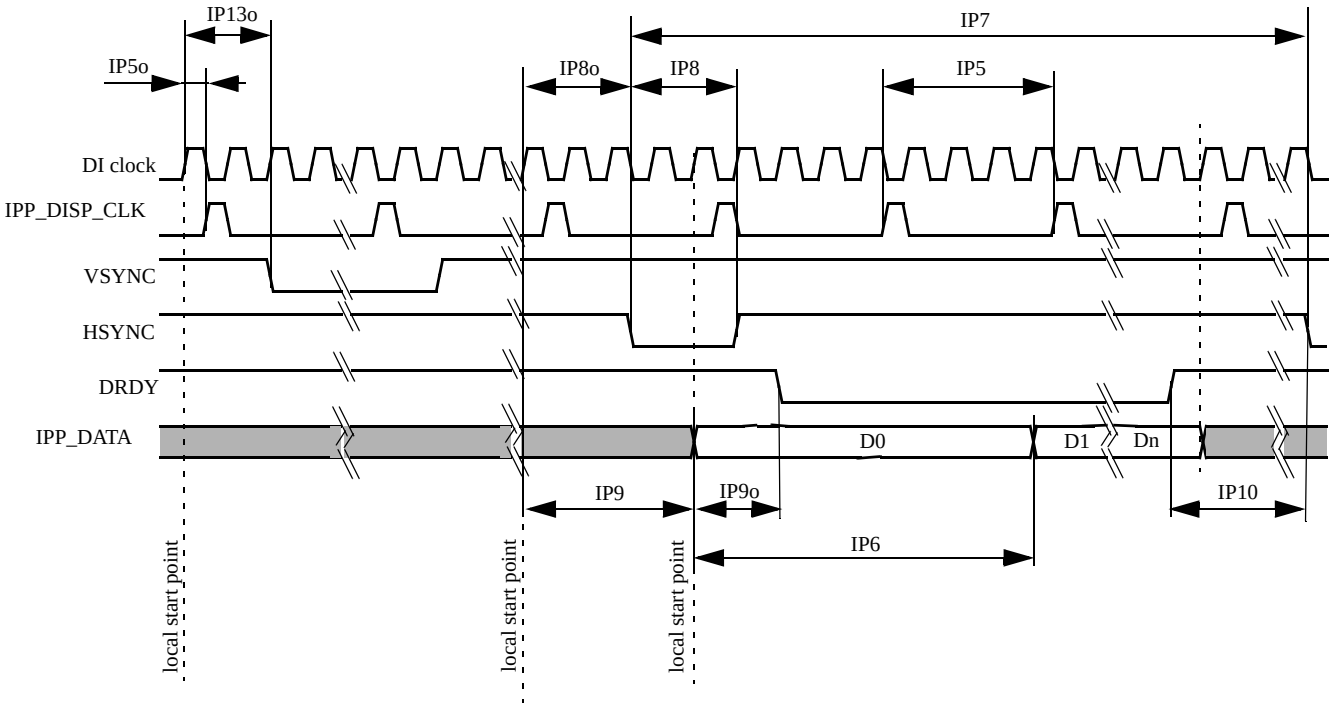


Figure 66. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 67 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

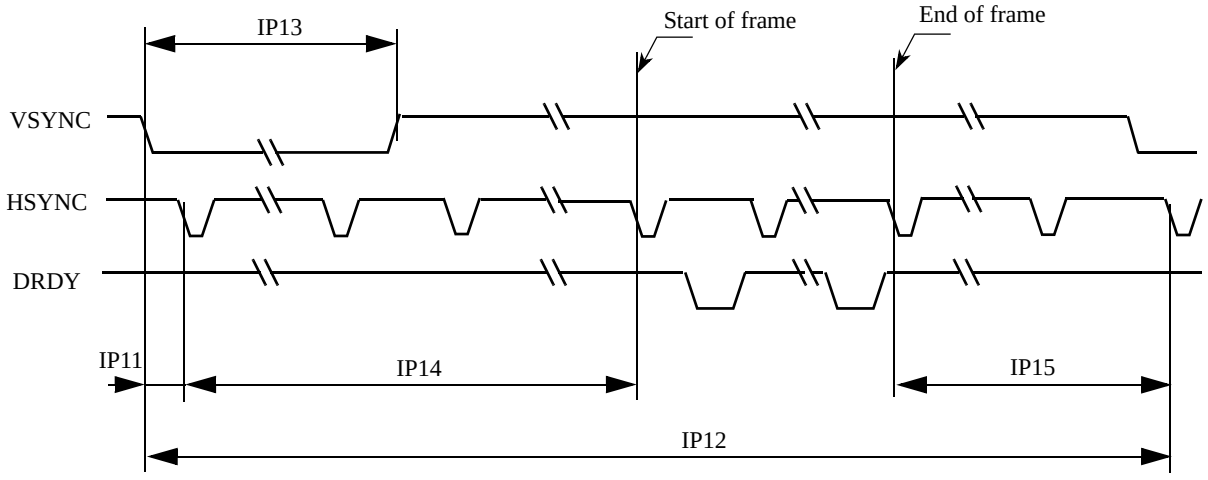


Figure 67. TFT Panels Timing Diagram—Vertical Sync Pulse

Table 68 shows timing characteristics of signals presented in Figure 66 and Figure 67.

Table 68. Synchronous Display Interface Timing Characteristics (Pixel Level)

ID	Parameter	Symbol	Value	Description	Unit
IP5	Display interface clock period	Tdicp	([1])	Display interface clock. IPP_DISP_CLK	ns
IP6	Display pixel clock period	Tdpcp	DISP_CLK_PER_PIXEL × Tdicp	Time of translation of one pixel to display, DISP_CLK_PER_PIXEL—number of pixel components in one pixel (1.n). The DISP_CLK_PER_PIXEL is virtual parameter to define Display pixel clock period. The DISP_CLK_PER_PIXEL is received by DC/DI one access division to **n** components.	ns
IP7	Screen width time	Tsw	(SCREEN_WIDTH) × Tdicp	SCREEN_WIDTH—screen width in, interface clocks. horizontal blanking included. The SCREEN_WIDTH should be built by suitable DI's counter[2].	ns
IP8	HSYNC width time	Thsw	(HSYNC_WIDTH)	HSYNC_WIDTH—Hsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter.	ns
IP9	Horizontal blank interval 1	Thbi1	BGXP × Tdicp	BGXP—width of a horizontal blanking before a first active data in a line (in interface clocks). The BGXP should be built by suitable DI's counter.	ns
IP10	Horizontal blank interval 2	Thbi2	(SCREEN_WIDTH – BGXP – FW) × Tdicp	Width a horizontal blanking after a last active data in a line (in interface clocks) FW—with of active line in interface clocks. The FW should be built by suitable DI's counter.	ns
IP12	Screen height	Tsh	(SCREEN_HEIGHT) × Tsw	SCREEN_HEIGHT— screen height in lines with blanking. The SCREEN_HEIGHT is a distance between 2 VSYNCs. The SCREEN_HEIGHT should be built by suitable DI's counter.	ns
IP13	VSYNC width	Tvsw	VSYNC_WIDTH	VSYNC_WIDTH—Vsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter	ns
IP14	Vertical blank interval 1	Tvbi1	BGYP × Tsw	BGYP—width of first Vertical blanking interval in line. The BGYP should be built by suitable DI's counter.	ns
IP15	Vertical blank interval 2	Tvbi2	(SCREEN_HEIGHT – BGYP – FH) × Tsw	Width of second Vertical blanking interval in line. The FH should be built by suitable DI's counter.	ns

Table 68. Synchronous Display Interface Timing Characteristics (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP5o	Offset of IPP_DISP_CLK	Todicp	DISP_CLK_OFFSET × Tdiclk	DISP_CLK_OFFSET—offset of IPP_DISP_CLK edges from local start point, in DI_CLK×2 (0.5 DI_CLK Resolution). Defined by DISP_CLK counter	ns
IP13o	Offset of VSYNC	Tovs	VSYNC_OFFSET × Tdiclk	VSYNC_OFFSET—offset of Vsync edges from a local start point, when a Vsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The VSYNC_OFFSET should be built by suitable DI's counter.	ns
IP8o	Offset of HSYNC	Tohs	HSYNC_OFFSET × Tdiclk	HSYNC_OFFSET—offset of Hsync edges from a local start point, when a Hsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The HSYNC_OFFSET should be built by suitable DI's counter.	ns
IP9o	Offset of DRDY	Todrdy	DRDY_OFFSET × Tdiclk	DRDY_OFFSET—offset of DRDY edges from a suitable local start point, when a corresponding data has been set on the bus, in DI_CLK×2 (0.5 DI_CLK Resolution). The DRDY_OFFSET should be built by suitable DI's counter.	ns

[1] Display interface clock period immediate value.

$$Tdicp = \begin{cases} T_{diclk} \times \dfrac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}, & \text{for integer } \dfrac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD} \\ T_{diclk}\left(floor\left[\dfrac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}\right] + 0.5 \pm 0.5\right), & \text{for fractional } \dfrac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD} \end{cases}$$

DISP_CLK_PERIOD—number of DI_CLK per one Tdicp. Resolution 1/16 of DI_CLK.
DI_CLK_PERIOD—relation of between programing clock frequency and current system clock frequency
Display interface clock period average value.

$$\overline{T}dicp = T_{diclk} \times \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}$$

[2] DI's counter can define offset, period and UP/DOWN characteristic of output signal according to programed parameters of the counter. Same of parameters in the table are not defined by DI's registers directly (by name), but can be generated by corresponding DI's counter. The SCREEN_WIDTH is an input value for DI's HSYNC generation counter. The distance between HSYNCs is a SCREEN_WIDTH.

The maximal accuracy of UP/DOWN edge of controls is:

$$Accuracy = (0.5 \times T_{diclk}) \pm 0.62ns$$

The maximal accuracy of UP/DOWN edge of IPP_DATA is:

$$Accuracy = T_{diclk} \pm 0.62ns$$

The DISP_CLK_PERIOD, DI_CLK_PERIOD parameters are programmed through the registers.

Figure 68 depicts the synchronous display interface timing for access level. The DISP_CLK_DOWN and DISP_CLK_UP parameters are set through the Register. Table 69 lists the synchronous display interface timing characteristics.

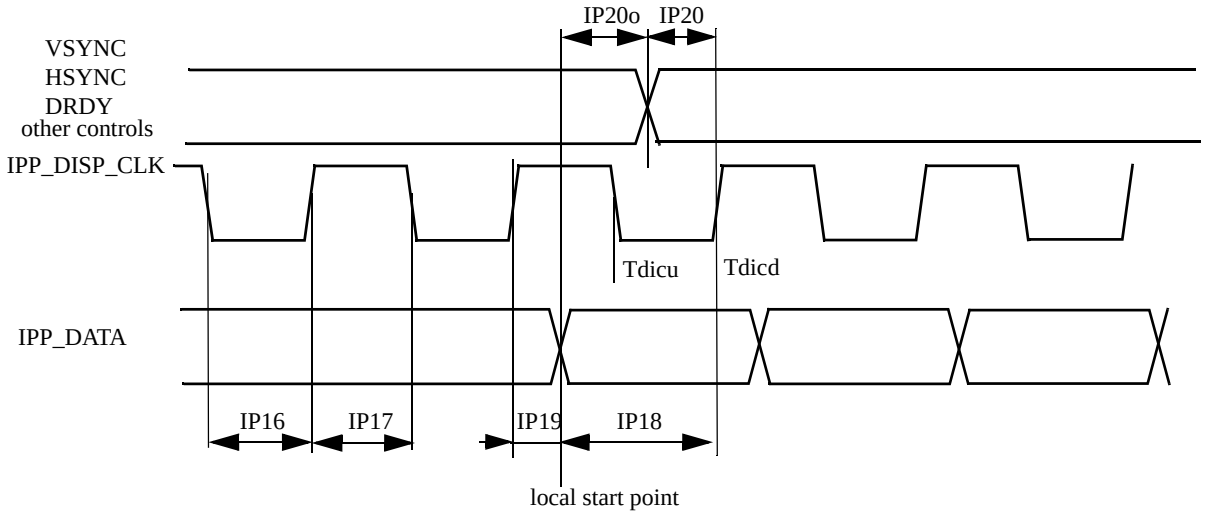


Figure 68. Synchronous Display Interface Timing Diagram—Access Level

Table 69. Synchronous Display Interface Timing Characteristics (Access Level)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP16	Display interface clock low time	Tckl	Tdicd-Tdicu-1.24	Tdicd[2]-Tdicu[3]	Tdicd-Tdicu+1.24	ns
IP17	Display interface clock high time	Tckh	Tdicp-Tdicd+Tdicu-1.24	Tdicp-Tdicd+Tdicu	Tdicp-Tdicd+Tdicu+1.2	ns
IP18	Data setup time	Tdsu	Tdicd-1.24	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp-Tdicd-1.24	Tdicp-Tdicu	—	ns
IP20o	Control signals offset times (defines for each pin)	Tocsu	Tocsu-1.24	Tocsu	Tocsu+1.24	ns
IP20	Control signals setup time to display interface clock (defines for each pin)	Tcsu	Tdicd-1.24-Tocsu%Tdicp	Tdicu	—	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

[2] Display interface clock down time

$$Tdicd = \frac{1}{2}\left(T_{diclk} \times ceil\left[\frac{2 \times DISP\_CLK\_DOWN}{DI\_CLK\_PERIOD}\right]\right)$$

[3] Display interface clock up time where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

$$Tdicu = \frac{1}{2}\left(T_{diclk} \times ceil\left[\frac{2 \times DISP\_CLK\_UP}{DI\_CLK\_PERIOD}\right]\right)$$

4.11.10.7 Asynchronous Interfaces

The following sections describes the types of asynchronous interfaces.

4.11.10.7.1 Standard Parallel Interfaces

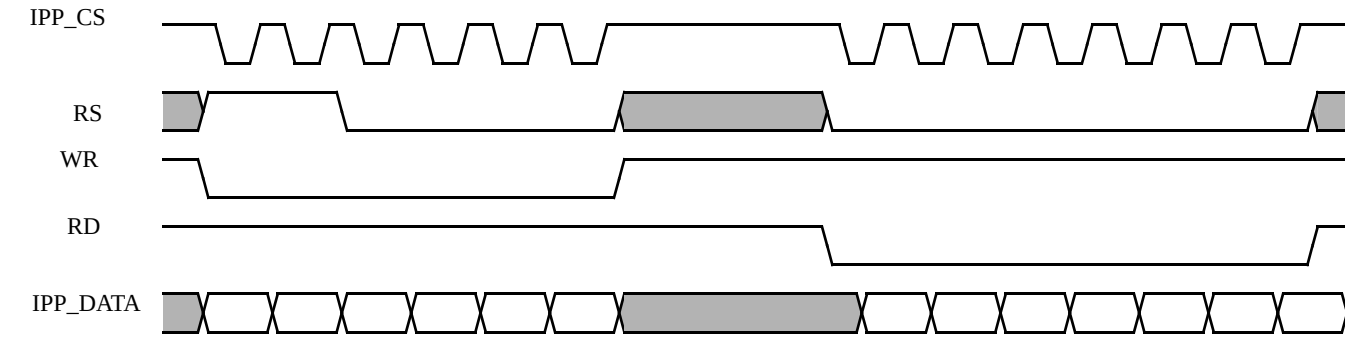
The IPU has four signal generator machines for asynchronous signal. Each machine generates IPU's internal control levels (0 or 1) by UP and DOWN that are defined in registers. Each asynchronous pin has a dynamic connection with one of the signal generators. This connection is redefined again with a new display access (pixel/component). The IPU can generate control signals according to system 80/68 requirements. The burst length is received as a result from predefined behavior of the internal signal generator machines.

The access to a display is realized by the following:

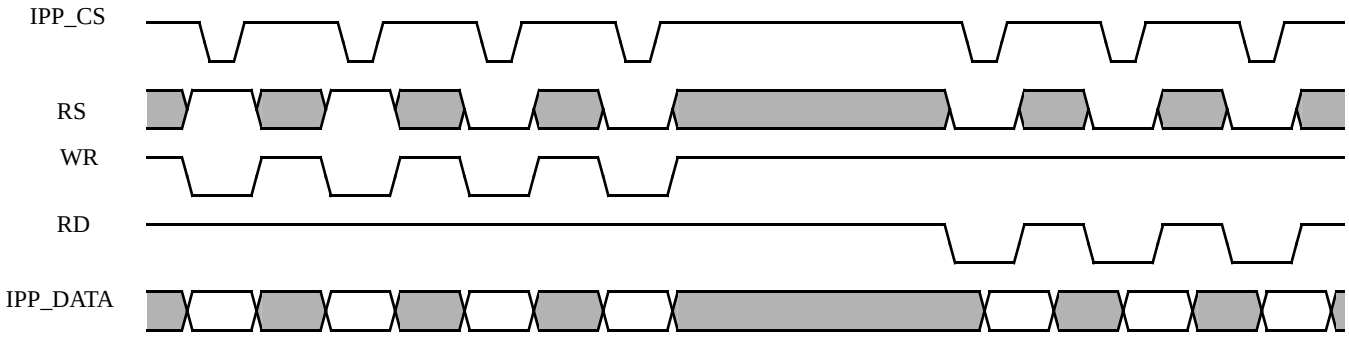
- CS (IPP_CS) chip select
- WR (IPP_PIN_11) write strobe
- RD (IPP_PIN_12) read strobe
- RS (IPP_PIN_13) Register select (A0)

Both system 80 and system 68k interfaces are supported for all described modes as depicted in Figure 69, Figure 70, Figure 71, and Figure 72. The timing images correspond to active-low IPP_CS, WR and RD signals.

Each asynchronous access is defined by an access size parameter. This parameter can be different between different kinds of accesses. This parameter defines a length of windows, when suitable controls of the current access are valid. A pause between two different display accesses can be guaranteed by programing suitable access sizes. There are no minimal/maximal hold/setup times hard defined by DI. Each control signal can be switched at any time during access size.



Burst access mode with sampling by CS signal



Single access mode (all control signals are not active for one display interface clock after each display access)

Figure 69. Asynchronous Parallel System 80 Interface (Type 1) Timing Diagram

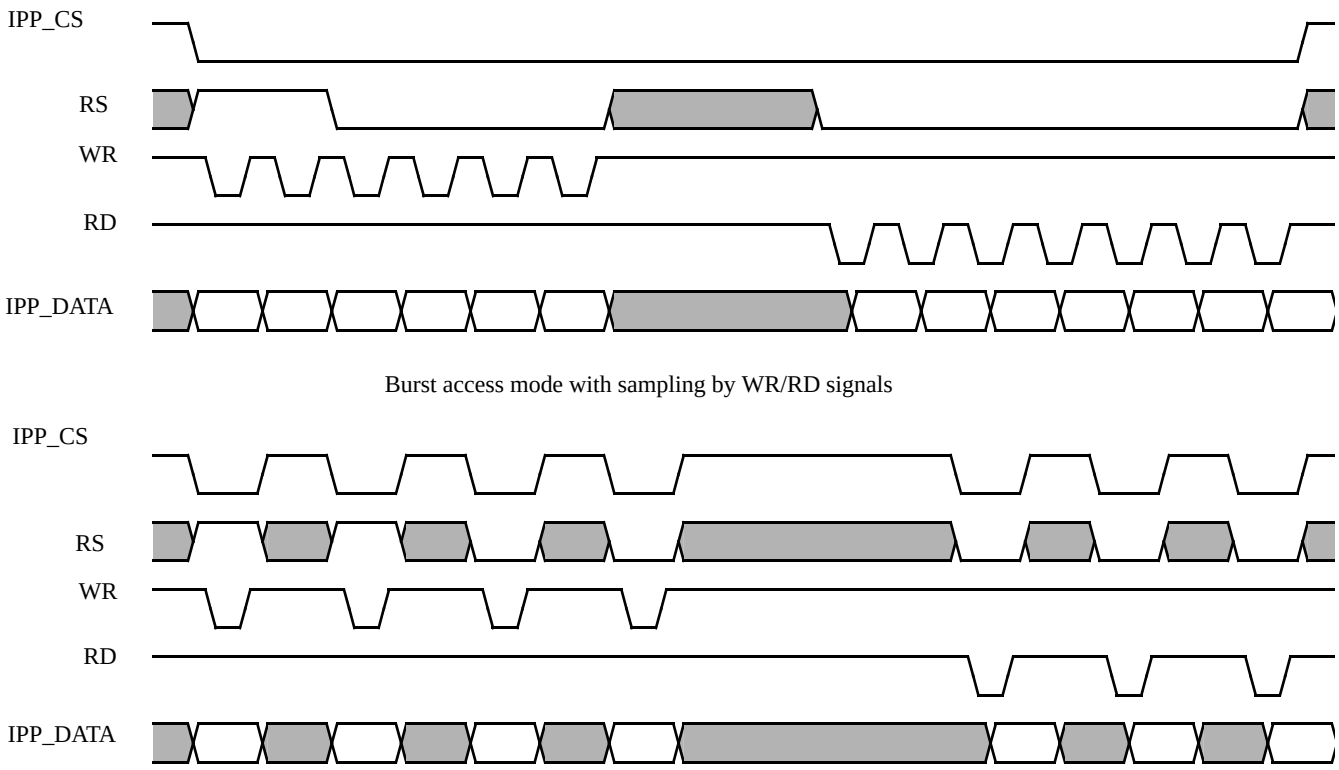


Figure 70. Asynchronous Parallel System 80 Interface (Type 2) Timing Diagram

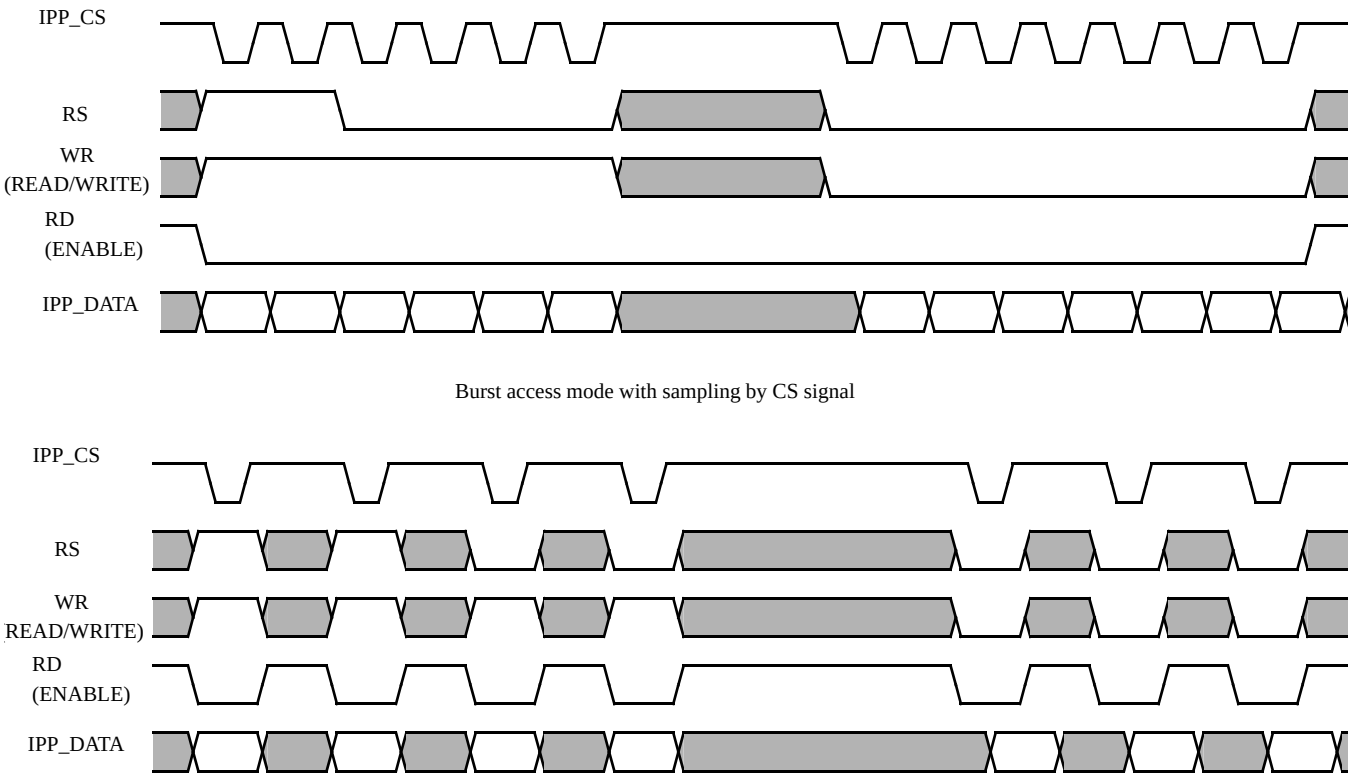


Figure 71. Asynchronous Parallel System 68k Interface (Type 1) Timing Diagram

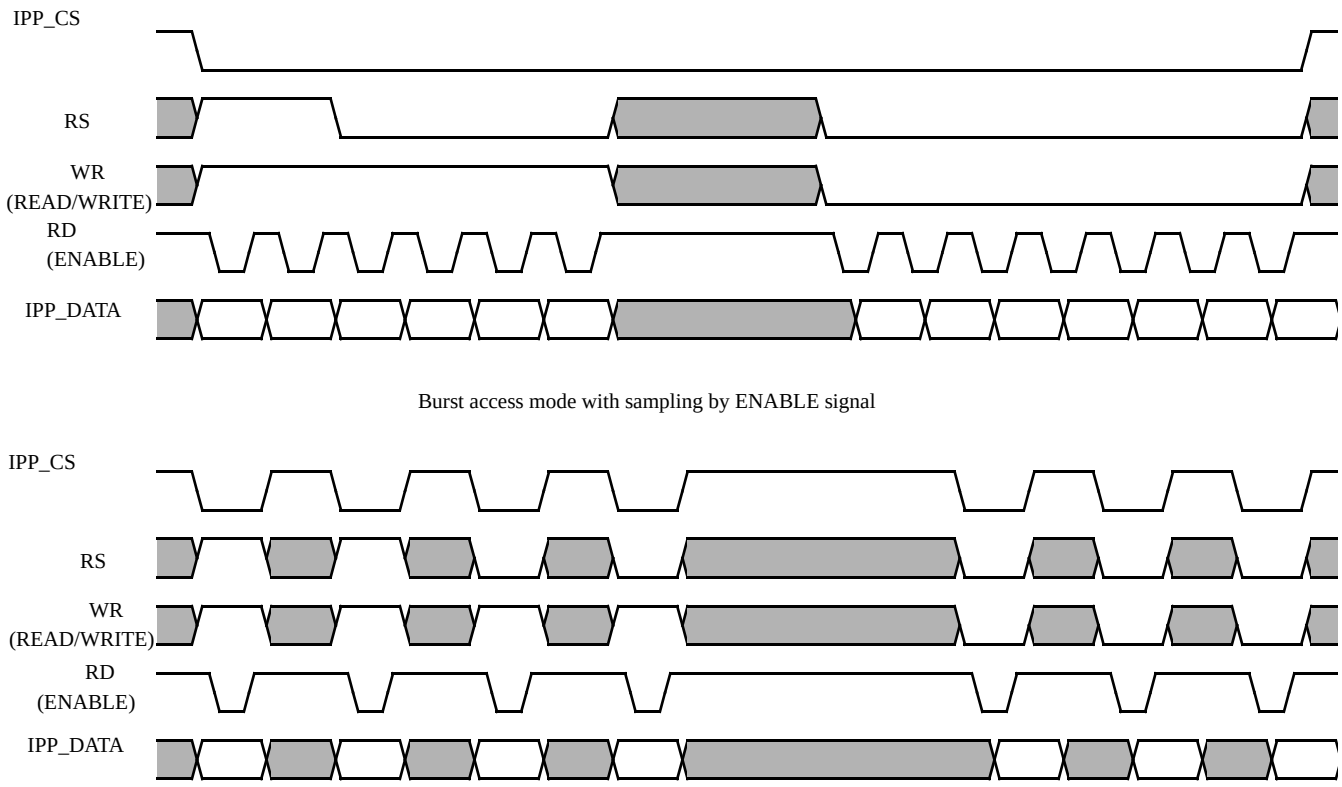


Figure 72. Asynchronous Parallel System 68k Interface (Type 2) Timing Diagram

Display operation can be performed with IPP_WAIT signal. The DI reacts to the incoming IPP_WAIT signal with 2 DI_CLK delay. The DI finishes a current access and a next access is postponed until IPP_WAIT release. Figure 73 shows timing of the parallel interface with IPP_WAIT control.

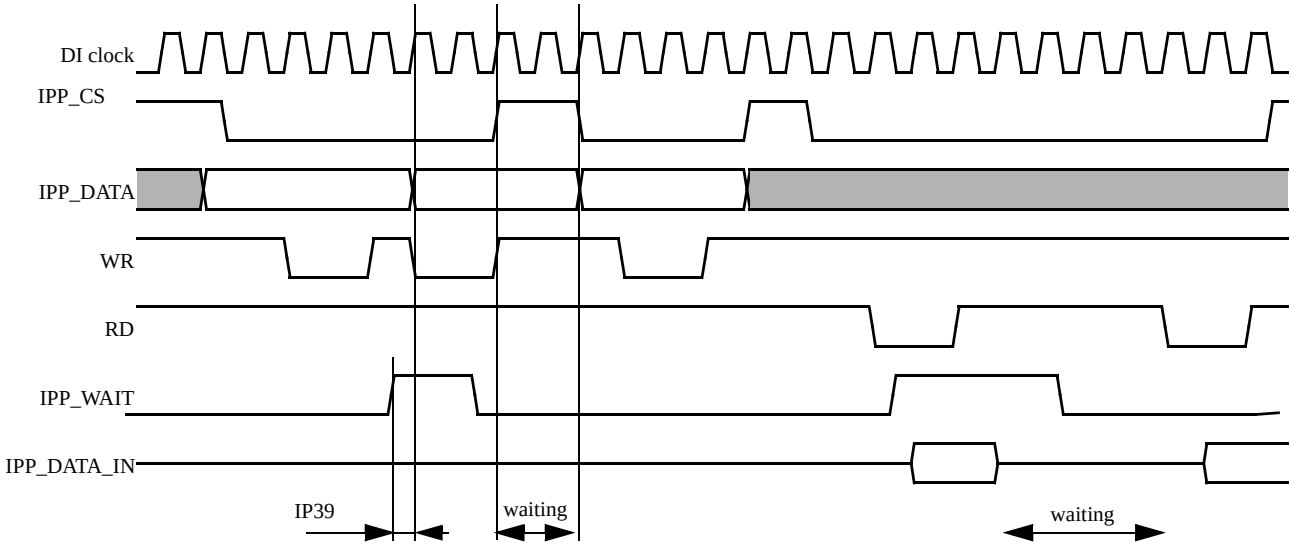


Figure 73. Parallel Interface Timing Diagram—Read Wait States

4.11.10.7.2 Asynchronous Parallel Interface Timing Parameters

Figure 74 depicts timing of asynchronous parallel interfaces based on the system 80 and system 68k interfaces. Table 71 shows timing characteristics at display access level. All timing diagrams are based on active low control signals (signals polarity is controlled through the DI_DISP_SIG_POL register).

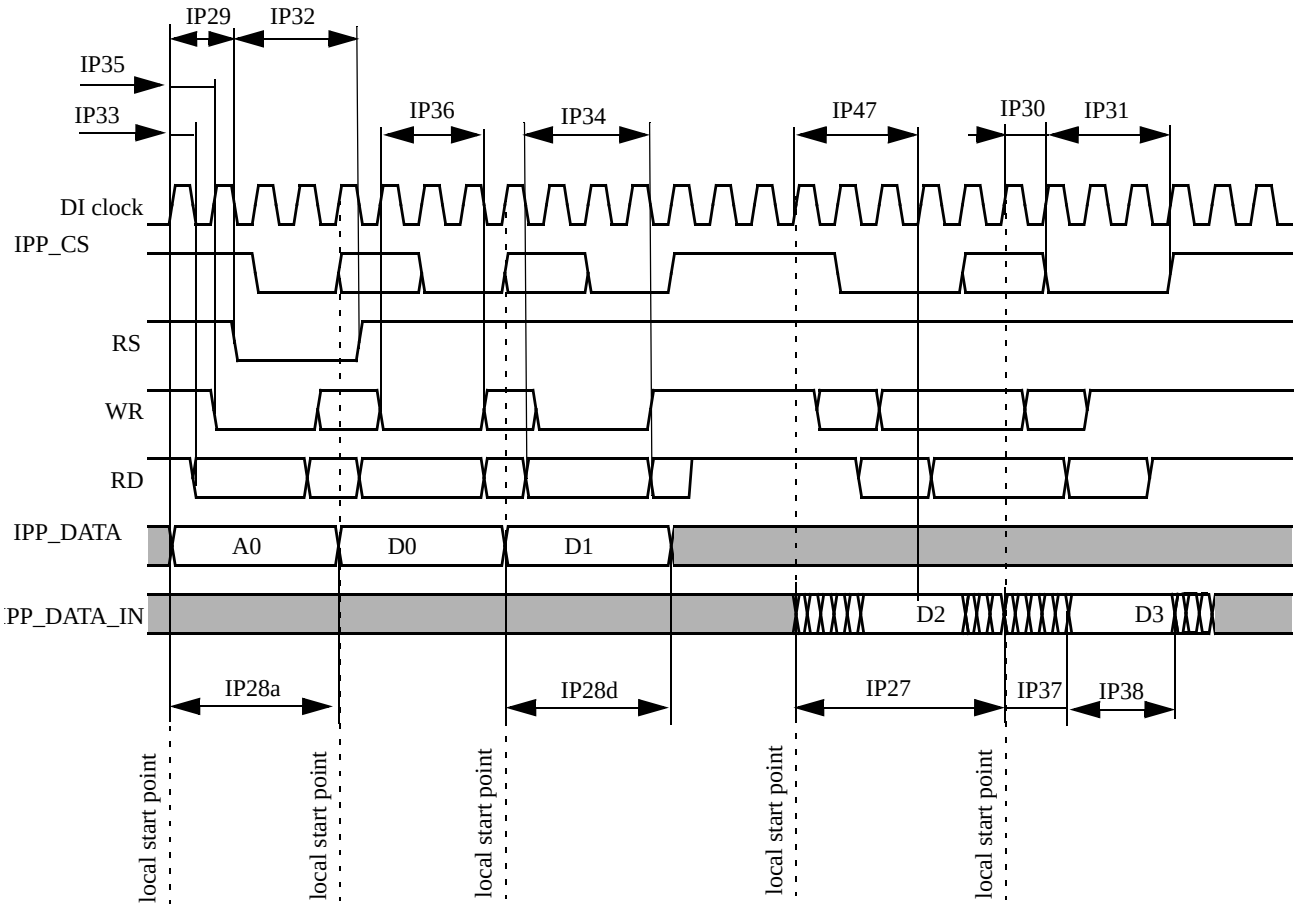


Figure 74. Asynchronous Parallel Interface Timing Diagram

Table 70. Asynchronous Display Interface Timing Parameters (Pixel Level)

ID	Parameter	Symbol	Value	Description	Unit
IP28a	Address Write system cycle time	Tcycwa	ACCESS_SIZE_#	Predefined value in DI REGISTER	ns
IP28d	Data Write system cycle time	Tcycwd	ACCESS_SIZE_#	Predefined value in DI REGISTER	ns
IP29	RS start	Tdcsrr	UP#	RS strobe switch, predefined value in DI REGISTER	ns
IP30	CS start	Tdcsc	UP#	CS strobe switch, predefined value in DI REGISTER	ns
IP31	CS hold	Tdchc	DOWN#	CS strobe release, predefined value in DI REGISTER	—
IP32	RS hold	Tdchrr	DOWN#	RS strobe release, predefined value in DI REGISTER	—
IP35	Write start	Tdcsw	UP#	Write strobe switch, predefined value in DI REGISTER	ns

Table 70. Asynchronous Display Interface Timing Parameters (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP36	Controls hold time for write	Tdchw	DOWN#	Write strobe release, predefined value in DI REGISTER	ns
IP37	Slave device data delay[1]	Tracc	Delay of incoming data	Physical delay of display's data, defined from Read access local start point	ns
IP38	Slave device data hold time	Troh	Hold time of data on the buss	Time that display read data is valid in input bus	ns

[1]This parameter is a requirement to the display connected to the IPU.

Table 71. Asynchronous Parallel Interface Timing Parameters (Access Level)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP28	Write system cycle time	Tcycw	Tdicpw – 1.24	Tdicpw[2]	Tdicpw+1.24	ns
IP29	RS start	Tdcsrr	Tdicurs – 1.24	Tdicurs	Tdicurs+1.24	ns
IP30	CS start	Tdcsc	Tdicucs – 1.24	Tdicur	Tdicucs+1.24	ns
IP31	CS hold	Tdchc	Tdicdcs – Tdicucs – 1.24	Tdicdcs[3]–Tdicucs[4]	Tdicdcs – Tdicucs+1.24	ns
IP32	RS hold	Tdchrr	Tdicdrs – Tdicurs – 1.24	Tdicdrs[5]–Tdicurs[6]	Tdicdrs – Tdicurs+1.24	ns
IP35	Controls setup time for write	Tdcsw	Tdicuw – 1.24	Tdicuw	Tdicuw+1.24	ns
IP36	Controls hold time for write	Tdchw	Tdicdw – Tdicuw – 1.24	Tdicpw[7]–Tdicuw[8]	Tdicdw–Tdicuw+1.24	ns
IP37	Slave device data delay[9]	Tracc	0	—	Tdrp[10] – Tlbd[11] –Tdicur–1.24	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

[2]Display period value for write

$$Tdicpw = T_{DI\_CLK} \times ceil\left[\frac{DI\_ACCESS\_SIZE\_\#}{DI\_CLK\_PERIOD}\right]$$

ACCESS_SIZE is predefined in REGISTER.

[3]Display control down for CS

$$Tdicdcs = \frac{1}{2}\left(T_{DI\_CLK} \times ceil\left[\frac{2 \times DISP\_DOWN\_\#}{DI\_CLK\_PERIOD}\right]\right)$$

DISP_DOWN is predefined in REGISTER.

[4]Display control up for CS

$$Tdicucs = \frac{1}{2}\left(T_{DI\_CLK} \times ceil\left[\frac{2 \times DISP\_UP\_\#}{DI\_CLK\_PERIOD}\right]\right)$$

DISP_UP is predefined in REGISTER.

[5]Display control down for RS

$$Tdicdrs = \frac{1}{2}\left(T_{DI\_CLK} \times ceil\left[\frac{2 \times DISP\_DOWN\_\#}{DI\_CLK\_PERIOD}\right]\right)$$

DISP_DOWN is predefined in REGISTER.

[6]Display control up for RS

$$Tdicurs = \frac{1}{2}\left(T_{DI\_CLK} \times ceil\left[\frac{2 \times DISP\_UP\_\#}{DI\_CLK\_PERIOD}\right]\right)$$

DISP_UP is predefined in REGISTER.

[7]Display control down for read

$$Tdicdrw = \frac{1}{2}\left(T_{DI\_CLK} \times ceil\left[\frac{2 \times DISP\_DOWN\_\#}{DI\_CLK\_PERIOD}\right]\right)$$

DISP_DOWN is predefined in REGISTER.

[8]Display control up for write

$$Tdicuw = \frac{1}{2}\left(T_{DI\_CLK} \times ceil\left[\frac{2 \times DISP\_UP\_\#}{DI\_CLK\_PERIOD}\right]\right)$$

DISP_UP is predefined in REGISTER.

[9]This parameter is a requirement to the display connected to the IPU.

[10]Data read point

$$Tdrp = T_{DI\_CLK} \times ceil\left[\frac{DISP\#\_READ\_EN}{DI\_CLK\_PERIOD}\right]$$

DISP#_READ_EN—operand of DC's MICROCDE READ command to sample incoming data.

[11]Loop back delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a chip-level output delay, board delays, a chip-level input delay, an IPU input delay. This value is chip specific.

4.11.11 LVDS Display Bridge (LDB) Module Parameters

The LVDS interface complies with TIA/EIA 644-A standard. For more details, see TIA/EIA STANDARD 644-A, "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits".

4.11.12 MIPI D-PHY Timing Parameters

This section describes MIPI D-PHY electrical specifications, compliant with MIPI CSI-2 version 1.0, D-PHY specification Rev. 1.0 (for MIPI sensor port x4 lanes) and MIPI DSI Version 1.01, and D-PHY specification Rev. 1.0 (and also DPI version 2.0, DBI version 2.0, DSC version 1.0a at protocol layer) (for MIPI display port x2 lanes).

4.11.12.1 Clock Multiplier Switching Characteristics

Table 72. Reference Clock Specifications

Symbol	Parameters	Test Conditions	Min	Max	Unit
F_{REFCLK}	REFCLK frequency	—	17	27	MHz

Table 72. Reference Clock Specifications (continued)

t_{CDC}	REFCLK duty cycle	—	40	60	%
J_{REFCLK}	REFCLK input phase noise	>1MHz offset	—	-120	dBc/Hz
Data and Control Interface Specifications					
t_{LPLL}	Lock Time	—	—	1	ms

4.11.12.2 Electrical and Timing Information

Table 73. Electrical and Timing Information

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
Input DC Specifications - Apply to CLKP/N and DATAP/N inputs						
V_I	Input signal voltage range	Transient voltage range is limited from -300 mV to 1600 mV	-50	—	1350	mV
V_{LEAK}	Input leakage current	VGNDSH(min) = VI = VGNDSH(max) + VOH(absmax) Lane module in LP Receive Mode	-10	—	10	mA
V_{GNDSH}	Ground Shift		-50	—	50	mV
$V_{OH(absmax)}$	Maximum transient output voltage level		—	—	1.45	V
$t_{voh(absmax)}$	Maximum transient time above VOH(absmax)		—	—	20	ns
HS Line Drivers DC Specifications						
$\|V_{OD}\|$	HS Transmit Differential output voltage magnitude	80 Ω<= RL< = 125 Ω	140	200	270	mV
$\Delta\|V_{OD}\|$	Change in Differential output voltage magnitude between logic states	80 Ω<= RL< = 125 Ω			10	mV
V_{CMTX}	Steady-state common-mode output voltage.	80 Ω<= RL< = 125 Ω	150	200	250	mV
$\Delta V_{CMTX}(1,0)$	Changes in steady-state common-mode output voltage between logic states	80 Ω<= RL< = 125 Ω			5	mV
V_{OHHS}	HS output high voltage	80 Ω<= RL< = 125 Ω			360	mV
Z_{OS}	Single-ended output impedance.		40	50	62.5	Ω
ΔZ_{OS}	Single-ended output impedance mismatch.				10	%
LP Line Drivers DC Specifications						

Table 73. Electrical and Timing Information (continued)

V_{OL}	Output low-level SE voltage		-50		50	mV
V_{OH}	Output high-level SE voltage		1.1	1.2	1.3	V
Z_{OLP}	Single-ended output impedance.		110			Ω
$\Delta Z_{OLP(01-10)}$	Single-ended output impedance mismatch driving opposite level				20	%
$\Delta Z_{OLP(0-11)}$	Single-ended output impedance mismatch driving same level				5	%
HS Line Receiver DC Specifications						
V_{IDTH}	Differential input high voltage threshold				70	mV
V_{IDTL}	Differential input low voltage threshold		-70			mV
V_{IHHS}	Single ended input high voltage				460	mV
V_{ILHS}	Single ended input low voltage		-40			mV
V_{CMRXDC}	Input common mode voltage		70		330	mV
Z_{ID}	Differential input impedance		80		125	Ω
LP Line Receiver DC Specifications						
V_{IL}	Input low voltage				550	mV
V_{IH}	Input high voltage		880			mV
V_{HYST}	Input hysteresis		25			mV
Contention Line Receiver DC Specifications						
V_{ILF}	Input low fault threshold		200		450	mV

4.11.12.3 D-PHY Signaling Levels

The signal levels are different for differential HS mode and single-ended LP mode. Figure 75 shows both the HS and LP signal levels on the left and right sides, respectively. The HS signaling levels are below the LP low-level input threshold such that LP receiver always detects low on HS signals.

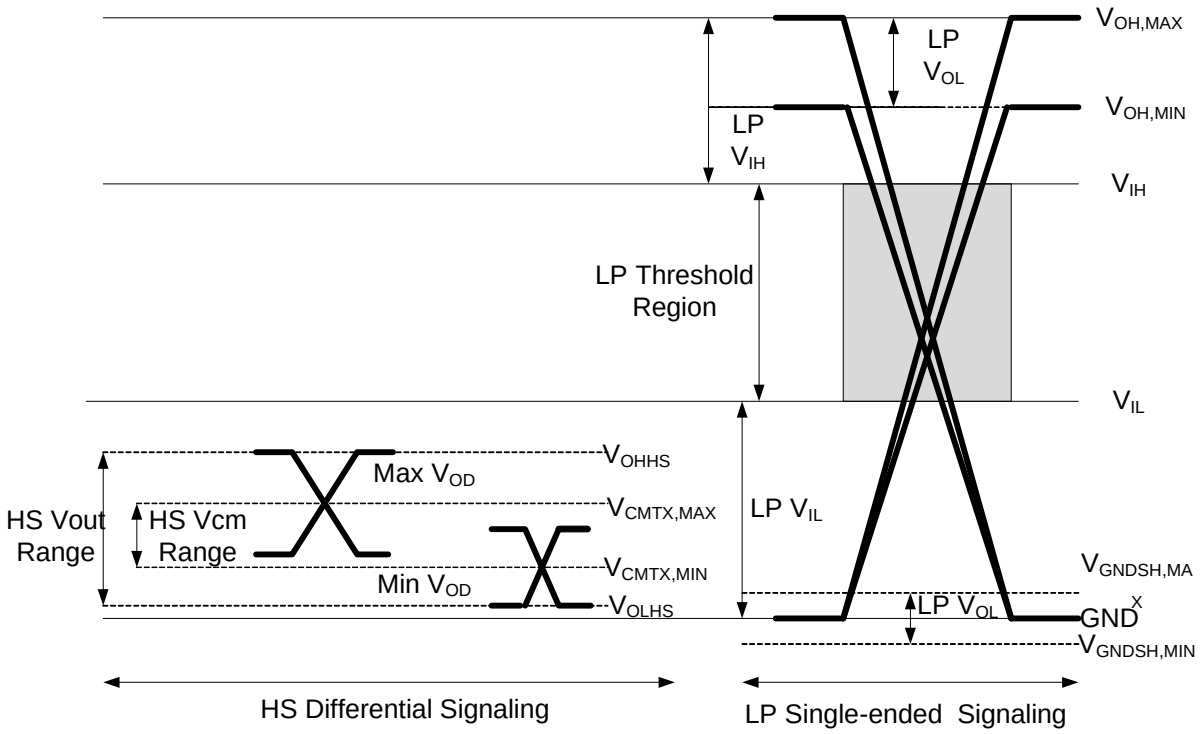


Figure 75. D-PHY Signaling Levels

4.11.12.4 HS Line Driver Characteristics

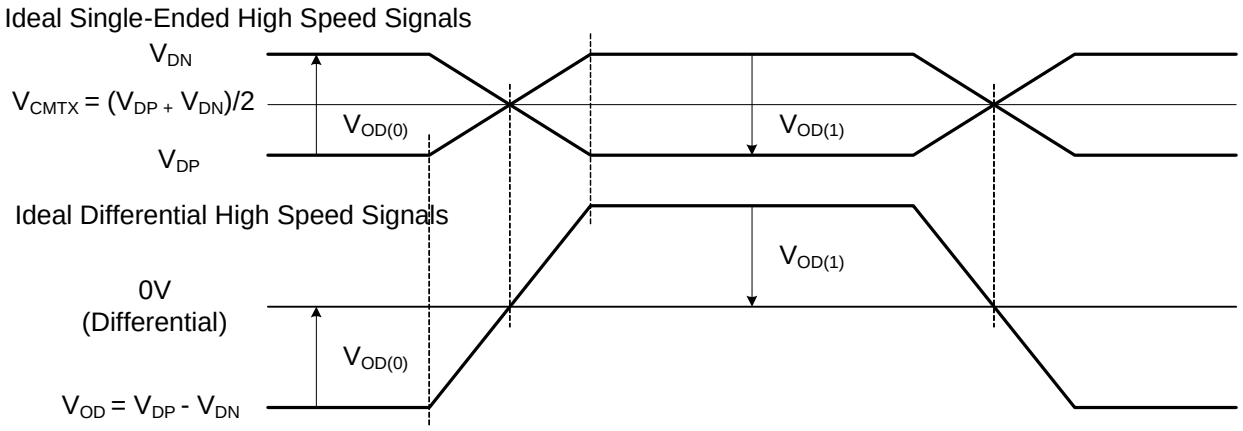


Figure 76. Ideal Single-ended and Resulting Differential HS Signals

4.11.12.5 Possible ΔVCMTX and ΔVOD Distortions of the Single-ended HS Signals

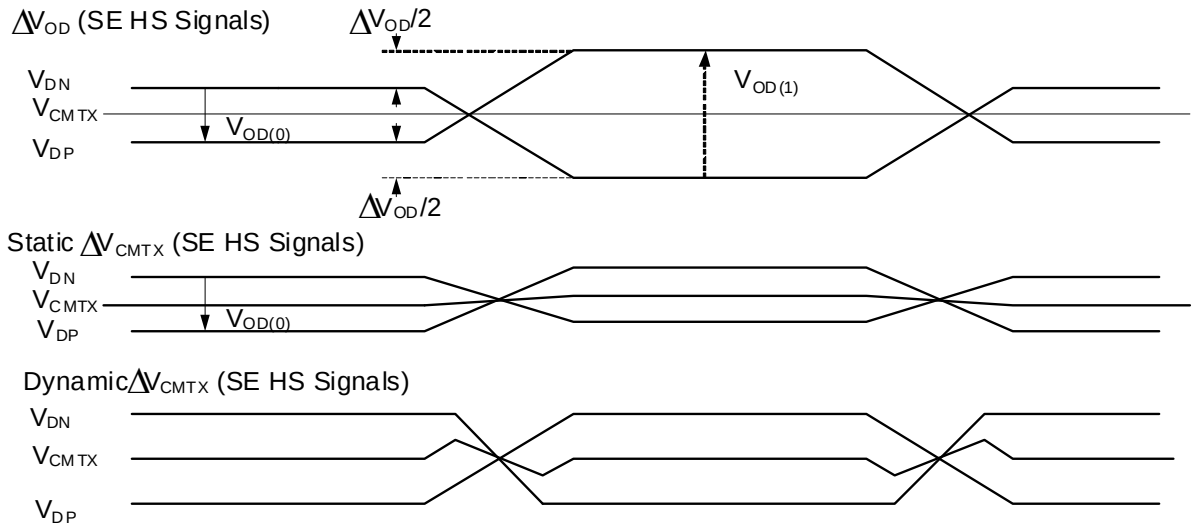


Figure 77. Possible ΔVCMTX and ΔVOD Distortions of the Single-ended HS Signals

4.11.12.6 D-PHY Switching Characteristics

Table 74. Electrical and Timing Information

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
Configuration clock						
F_{CFG_CLK}	CFG_CLK frequency		17	—	27	MHz
DC_{CFG_CLK}	CFG_CLK duty cycle		40	50	60	%
HS Line Drivers AC Specifications						
—	Maximum serial data rate (forward direction)	On DATAP/N outputs. 80 Ω <= RL <= 125 Ω	80	—	1000	Mbps
F_{DDRCLK}	DDR CLK frequency	On DATAP/N outputs.	40	—	500	MHz
P_{DDRCLK}	DDR CLK period	80 Ω <= RL< = 125 Ω	2	—	25	ns
t_{CDC}	DDR CLK duty cycle	$t_{CDC} = t_{CPH} / P_{DDRCLK}$	—	50	—	%
t_{CPH}	DDR CLK high time		—	1	—	UI
t_{CPL}	DDR CLK low time		—	1	—	UI
—	DDR CLK / DATA Jitter		—	75	—	ps pk-pk
$t_{SKEW[PN]}$	Intra-Pair (Pulse) skew			0.075		UI
$t_{SKEW[TX]}$	Data to Clock Skew		0.350		0.650	UI
$t_{SETUP[RX]}$	Data to Clock Receiver Setup time		0.15			UI

Table 74. Electrical and Timing Information

$t_{HOLD[RX]}$	Clock to Data Receiver Hold time		0.15			UI
t_r	Differential output signal rise time	20% to 80%, RL = 50 Ω	150		0.3UI	ps
t_f	Differential output signal fall time	20% to 80%, RL = 50 Ω	150		0.3UI	ps
$\Delta V_{CMTX(HF)}$	Common level variation above 450 MHz	80 Ω<= RL< = 125 Ω			15	mV_{rms}
$\Delta V_{CMTX(LF)}$	Common level variation between 50 MHz and 450 MHz.	80 Ω<= RL< = 125 Ω			20	mV_p
LP Line Drivers AC Specifications						
t_{rlp},t_{flp}	Single ended output rise/fall time	15% to 85%, C_L<70 pF			25	ns
t_{reo}		30% to 85%, C_L<70 pF			35	ns
$\delta V/\delta t_{SR}$	Signal slew rate	15% to 85%, C_L<70 pF			120	mV/ns
C_L	Load capacitance		0		70	pF
HS Line Receiver AC Specifications						
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz				200	mVpp
$\Delta V_{CMRX(LF)}$	Common mode interference between 50 MHz and 450 MHz.		-50		50	mVpp
C_{CM}	Common mode termination		=		60	pF
LP Line Receiver AC Specifications						
e_{SPIKE}	Input pulse rejection				300	Vps
T_{MIN}	Minimum pulse response		50			ns
V_{INT}	Pk-to-Pk interference voltage				400	mV
f_{INT}	Interference frequency		450			MHz
Model Parameters used for Driver Load switching performance evaluation						
C_{PAD}	Equivalent Single ended I/O PAD capacitance.				1	pF
C_{PIN}	Equivalent Single ended Package + PCB capacitance.				2	pF
L_S	Equivalent wire bond series inductance				1.5	nH

Table 74. Electrical and Timing Information

R_S	Equivalent wire bond series resistance				0.15	Ω
R_L	Load Resistance		80	100	125	Ω

4.11.12.7 High-Speed Clock Timing

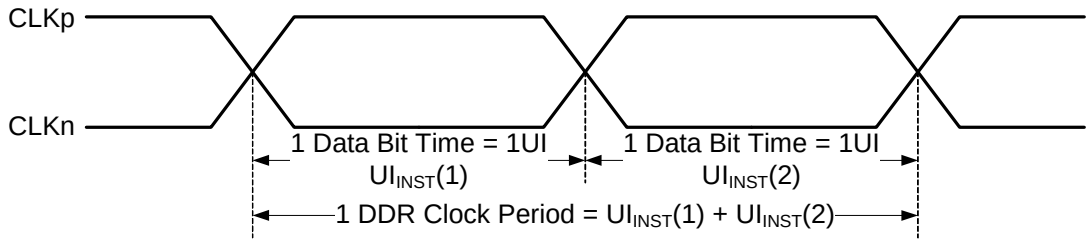


Figure 78. DDR Clock Definition

4.11.12.8 Forward High-Speed Data Transmission Timing

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 79:

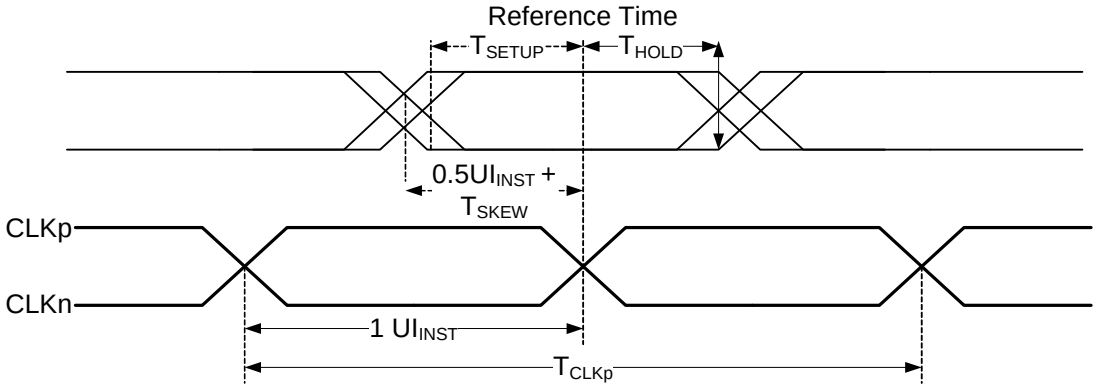


Figure 79. Data to Clock Timing Definitions

4.11.12.9 Reverse High-Speed Data Transmission Timing

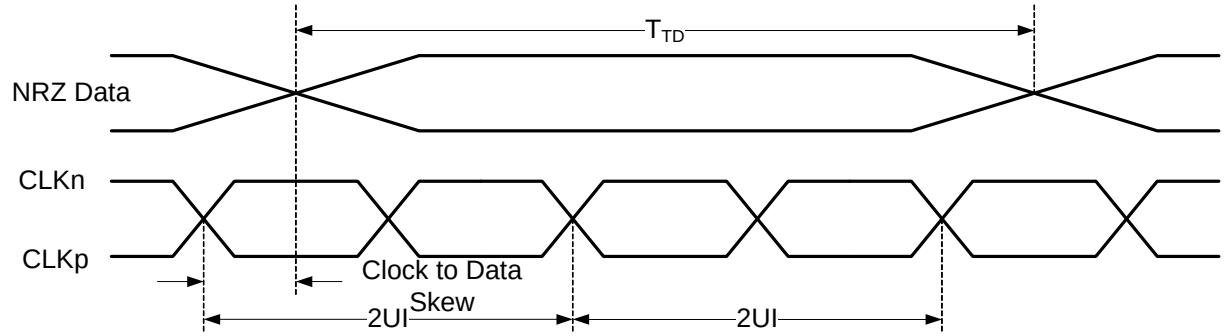


Figure 80. Reverse High-Speed Data Transmission Timing at Slave Side

4.11.12.10Low-Power Receiver Timing

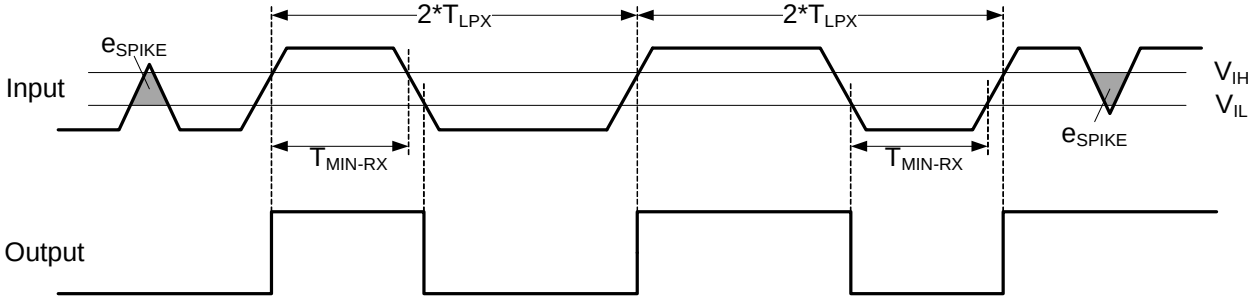


Figure 81. Input Glitch Rejection of Low-Power Receivers

4.11.13 HSI Host Controller Timing Parameters

This section describes the timing parameters of the HSI Host Controller which are compliant with High-Speed Synchronous Serial Interface (HSI) Physical Layer specification version1.01.

4.11.13.1 Synchronous Data Flow

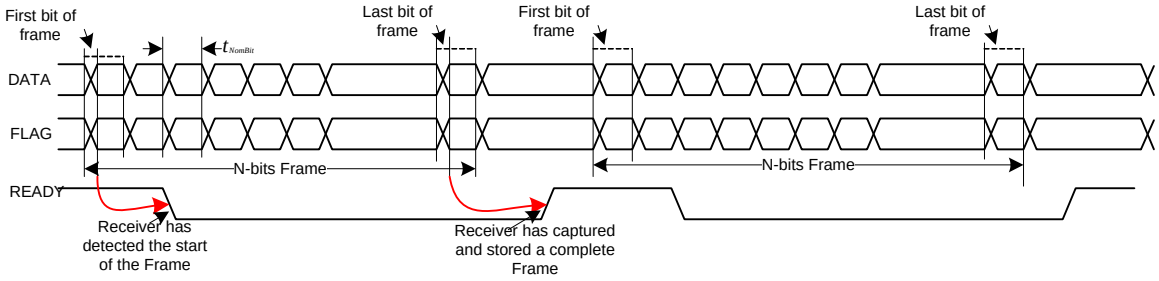


Figure 82. Synchronized Data Flow READY Signal Timing (Frame and Stream Transmission)

4.11.13.2 Pipelined Data Flow

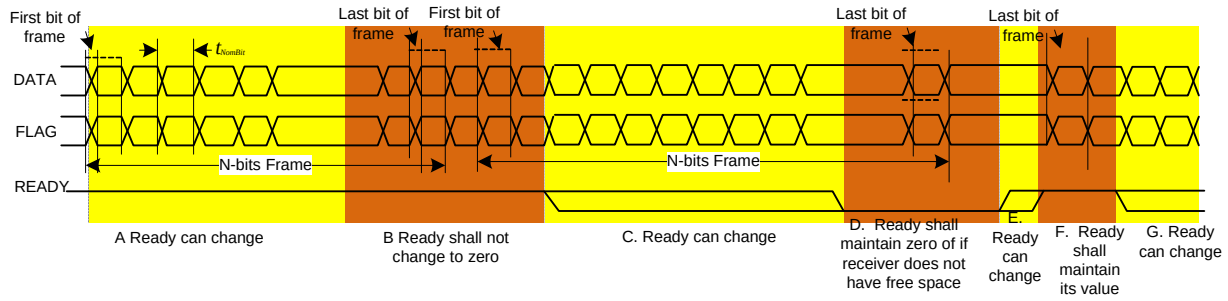


Figure 83. Pipelined Data Flow Ready Signal Timing (Frame Transmission Mode)

4.11.13.3 Receiver Real-Time Data Flow

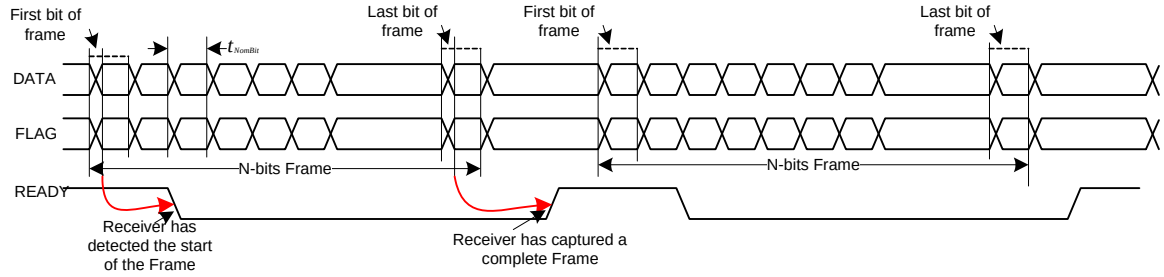


Figure 84. Receiver Real-Time Data Flow READY Signal Timing

4.11.13.4 Synchronized Data Flow Transmission with Wake

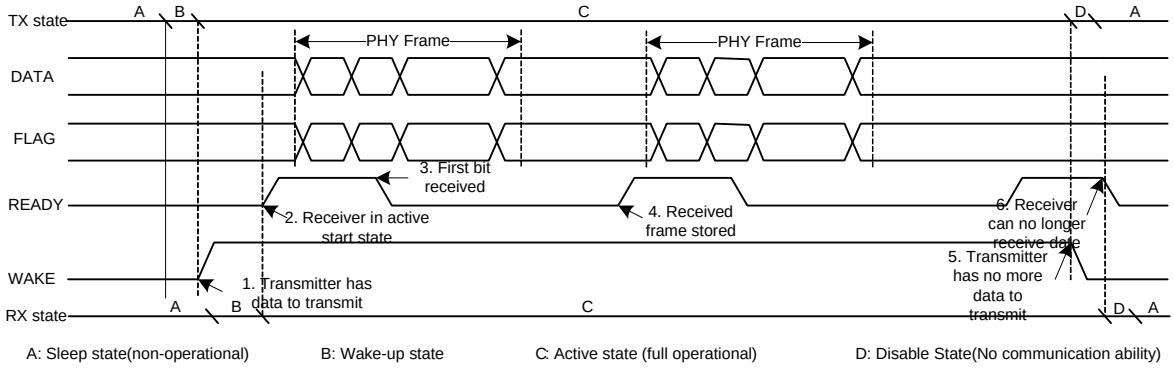


Figure 85. Synchronized Data Flow Transmission with WAKE

4.11.13.5 Stream Transmission Mode Frame Transfer

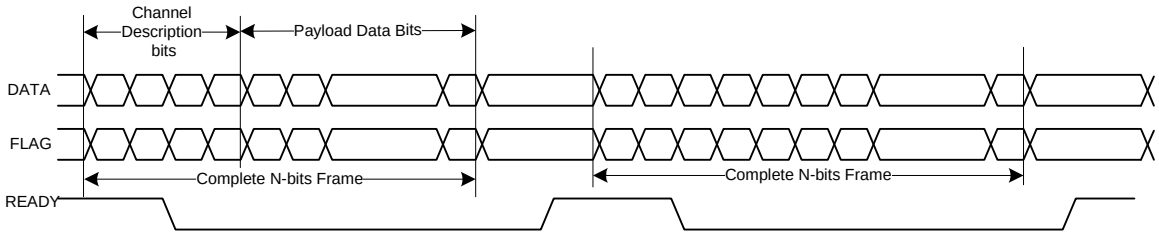


Figure 86. Stream Transmission Mode Frame Transfer (Synchronized Data Flow)

4.11.13.6 Frame Transmission Mode (Synchronized Data Flow)

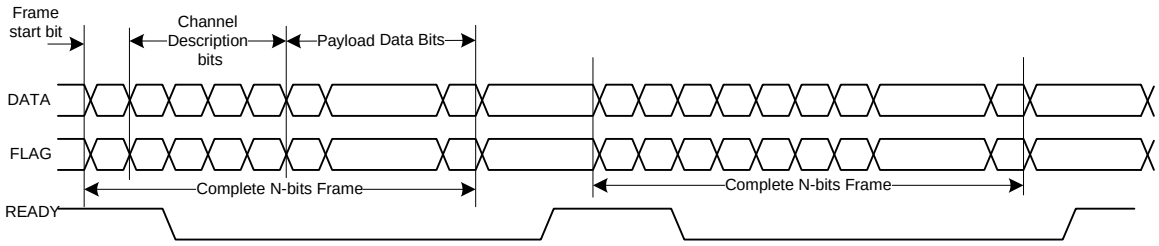


Figure 87. Frame Transmission Mode Transfer of Two Frames (Synchronized Data Flow)

4.11.13.7 Frame Transmission Mode (Pipelined Data Flow)

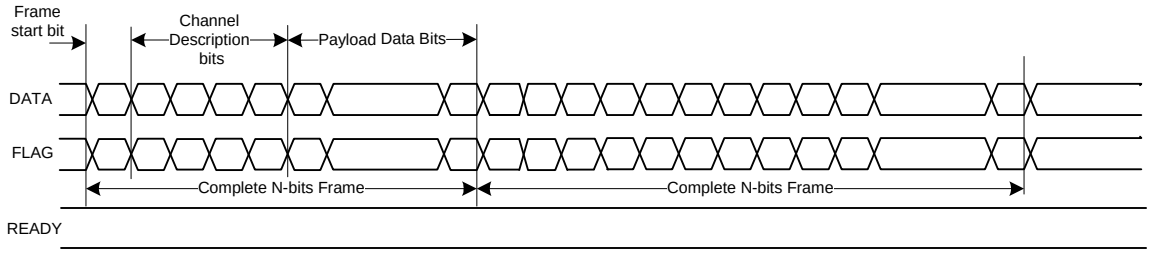


Figure 88. Frame Transmission Mode Transfer of Two Frames (Pipelined Data Flow)

4.11.13.8 DATA and FLAG Signal Timing Requirement for a 15 pF Load

Table 75. DATA and FLAG Timing

Parameter	Description	1 Mbit/s	100 Mbit/s	200 Mbit/s
$t_{Bit, nom}$	Nominal bit time	1000 ns	10.0 ns	5.00 ns
$t_{Rise, min}$ and $t_{Fall, min}$	Minimum allowed rise and fall time	2.00 ns	2.00 ns	1.00 ns
$t_{TxToRxSkew, maxfq}$	Maximum skew between transmitter and receiver package pins	50.0 ns	0.5.0 ns	0.25 ns

Table 75. DATA and FLAG Timing (continued)

Parameter	Description	1 Mbit/s	100 Mbit/s	200 Mbit/s
$t_{EageSepTx, min}$	Minimum allowed separation of signal transitions at transmitter package pins, including all timing defects, for example, jitter and skew, inside the transmitter.	400 ns	4.00 ns	2.00 ns
$t_{EageSepRx, min}$	Minimum separation of signal transitions, measured at the receiver package pins, including all timing defects, for example, jitter and skew, inside the receiver.	350 ns	3.5 ns	1.75 ns

4.11.13.9 DATA and FLAG Signal Timing

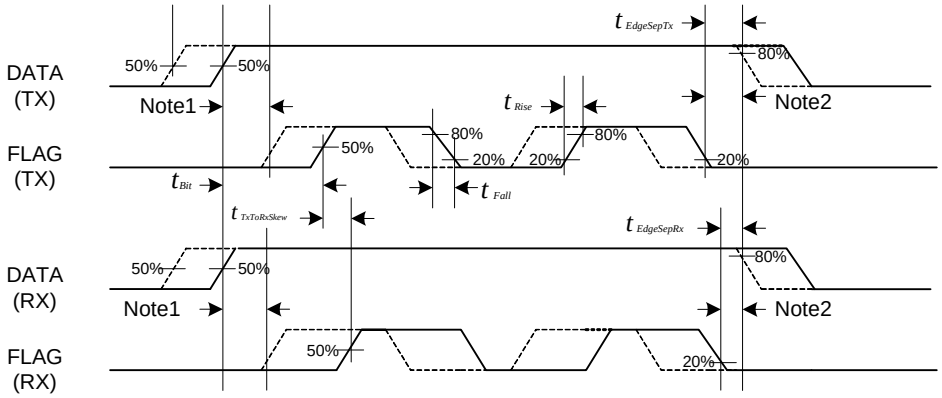


Figure 89. DATA and FLAG Signal Timing

4.11.14 PCIe PHY Parameters

The PCIe interface complies with PCIe specification Gen2 x1 lane and supports the PCI Express 1.1/2.0 standard.

4.11.14.1 PCIE_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 200 Ω. 1% precision resistor on PCIE_REXT pads to ground. It is used for termination impedance calibration.

4.11.15 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 90 depicts the timing of the PWM, and Table 76 lists the PWM timing parameters.

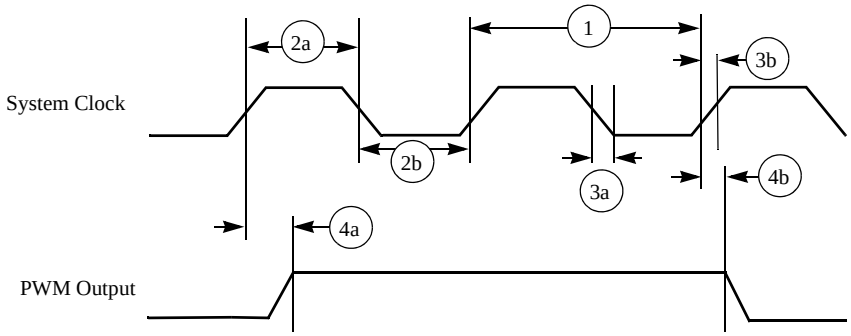


Figure 90. PWM Timing

Table 76. PWM Output Timing Parameters

Ref. No.	Parameter	Min	Max	Unit
1	System CLK frequency[1]	0	ipg_clk	MHz
2a	Clock high time	12.29	—	ns
2b	Clock low time	9.91	—	ns
3a	Clock fall time	—	0.5	ns
3b	Clock rise time	—	0.5	ns
4a	Output delay time	—	9.37	ns
4b	Output setup time	8.71	—	ns

[1] CL of PWMO = 30 pF

4.11.16 SATA PHY Parameters

This section describes SATA PHY electrical specifications.

4.11.16.1 Transmitter and Receiver Characteristics

The SATA PHY meets or exceeds the electrical compliance requirements defined in the SATA specifications.

NOTE

The tables in the following sections indicate any exceptions to the SATA specification or aspects of the SATA PHY that exceed the standard, as well as provide information about parameters not defined in the standard.

The following subsections provide values obtained from a combination of simulations and silicon characterization.

4.11.16.1.1 SATA PHY Transmitter Characteristics

Table 77 provides specifications for SATA PHY transmitter characteristics.

Table 77. SATA2 PHY Transmitter Characteristics

Parameters	Symbol	Min	Typ	Max	Unit
Transmit common mode voltage	V_{CTM}	0.4	—	0.6	V
Transmitter pre-emphasis accuracy (measured change in de-emphasized bit)	—	–0.5	—	0.5	dB

4.11.16.1.2 SATA PHY Receiver Characteristics

Table 78 provides specifications for SATA PHY receiver characteristics.

Table 78. SATA PHY Receiver Characteristics

Parameters	Symbol	Min	Typ	Max	Unit
Minimum Rx eye height (differential peak-to-peak)	$V_{MIN\_RX\_EYE\_HEIGHT}$	—	—	175	mV
Tolerance	PPM	–400	—	400	ppm

4.11.16.2 SATA_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 191 Ω 1% precision resistor on SATA_REXT pad to ground.

Resistor calibration consists of learning which state of the internal Resistor Calibration register causes an internal, digitally trimmed calibration resistor to best match the impedance applied to the SATA_REXT pin. The calibration register value is then supplied to all Tx and Rx termination resistors.

During the calibration process (for a few tens of microseconds), up to 0.3 mW can be dissipated in the external SATA_REXT resistor. At other times, no power is dissipated by the SATA_REXT resistor.

4.11.17 SCAN JTAG Controller (SJC) Timing Parameters

Figure 91 depicts the SJC test clock input timing. Figure 92 depicts the SJC boundary scan timing. Figure 93 depicts the SJC test access port. Signal parameters are listed in Table 79.

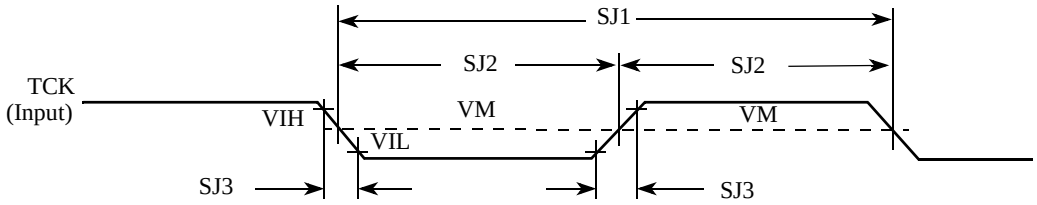


Figure 91. Test Clock Input Timing Diagram

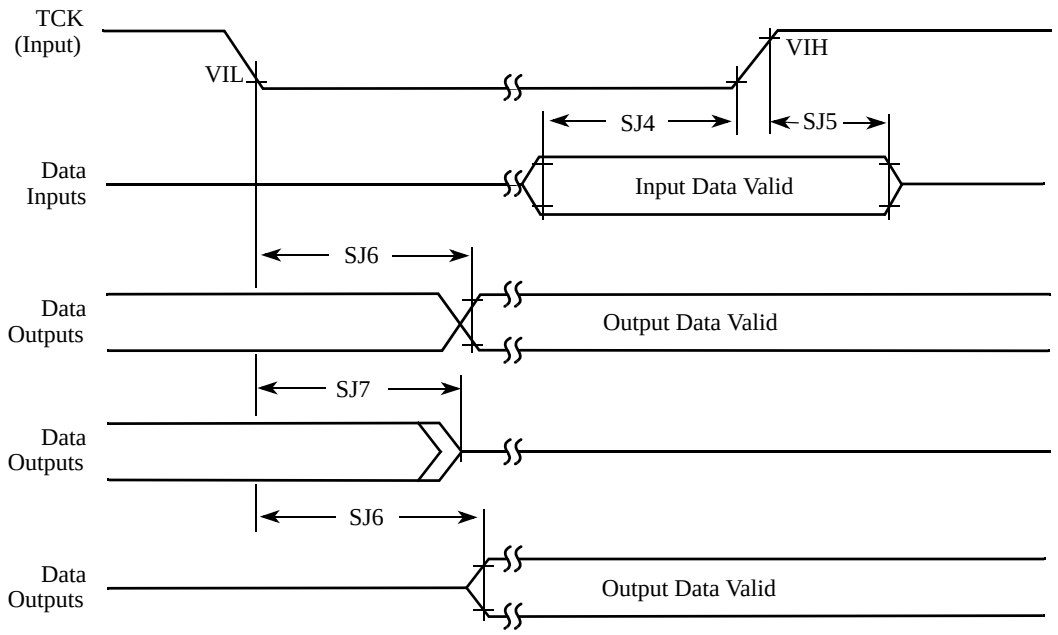


Figure 92. Boundary Scan (JTAG) Timing Diagram

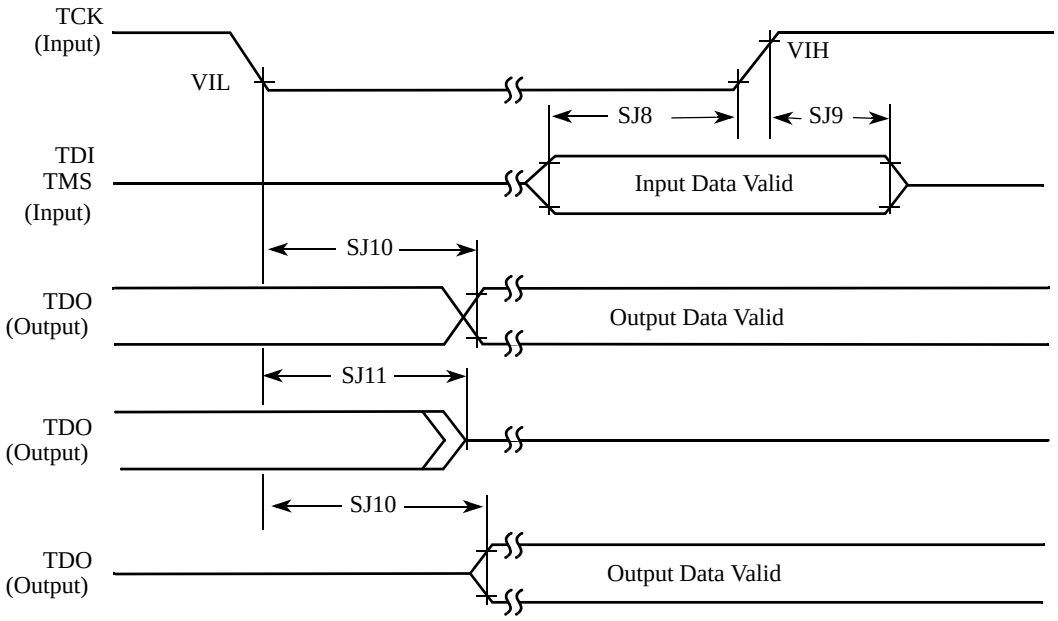


Figure 93. Test Access Port Timing Diagram

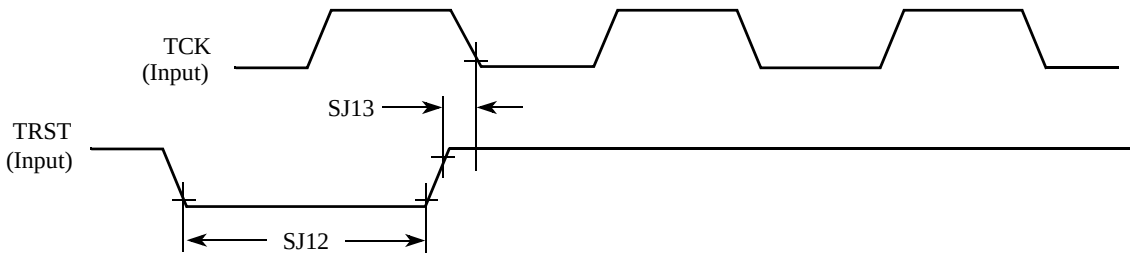


Figure 94. $\overline{\text{TRST}}$ Timing Diagram

Table 79. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	TCK frequency of operation $1/(3 \bullet T_{DC})$[1]	0.001	22	MHz
SJ1	TCK cycle time in crystal mode	45	—	ns
SJ2	TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	TCK low to output data valid	—	40	ns
SJ7	TCK low to output high impedance	—	40	ns
SJ8	TMS, TDI data set-up time	5	—	ns
SJ9	TMS, TDI data hold time	25	—	ns
SJ10	TCK low to TDO data valid	—	44	ns
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{\text{TRST}}$ assert time	100	—	ns
SJ13	$\overline{\text{TRST}}$ set-up time to TCK low	40	—	ns

1 T_{DC} = target frequency of SJC

2 V_M = mid-point voltage

4.11.18 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 80 and Figure 95 and Figure 96 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SRCK) for SPDIF in Rx mode and the timing of the modulating Tx clock (STCLK) for SPDIF in Tx mode.

Table 80. SPDIF Timing Parameters

Characteristics	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIFIN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIFOUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIFOUT1 output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SRCK) period	srckp	40.0	—	ns
SRCK high period	srckph	16.0	—	ns
SRCK low period	srckpl	16.0	—	ns
Modulating Tx clock (STCLK) period	stclkp	40.0	—	ns
STCLK high period	stclkph	16.0	—	ns
STCLK low period	stclkpl	16.0	—	ns

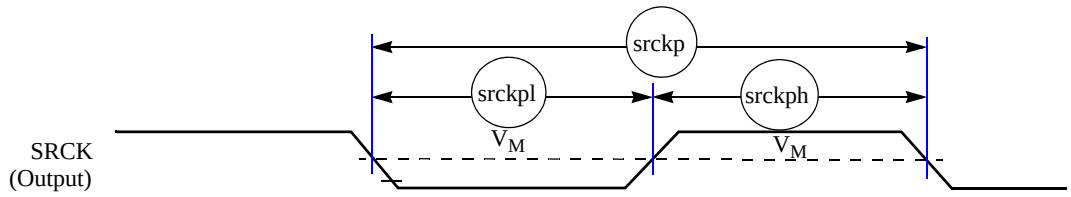


Figure 95. SRCK Timing Diagram

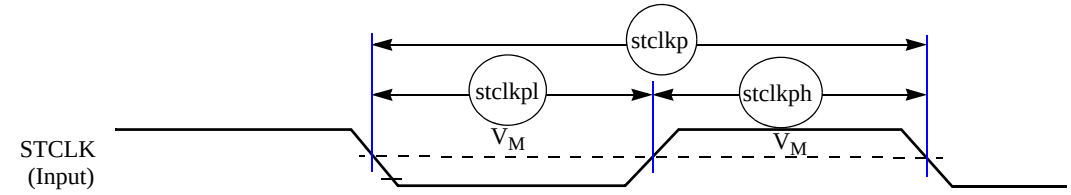


Figure 96. STCLK Timing Diagram

4.11.19 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces are summarized in Table 81.

Table 81. AUDMUX Port Allocation

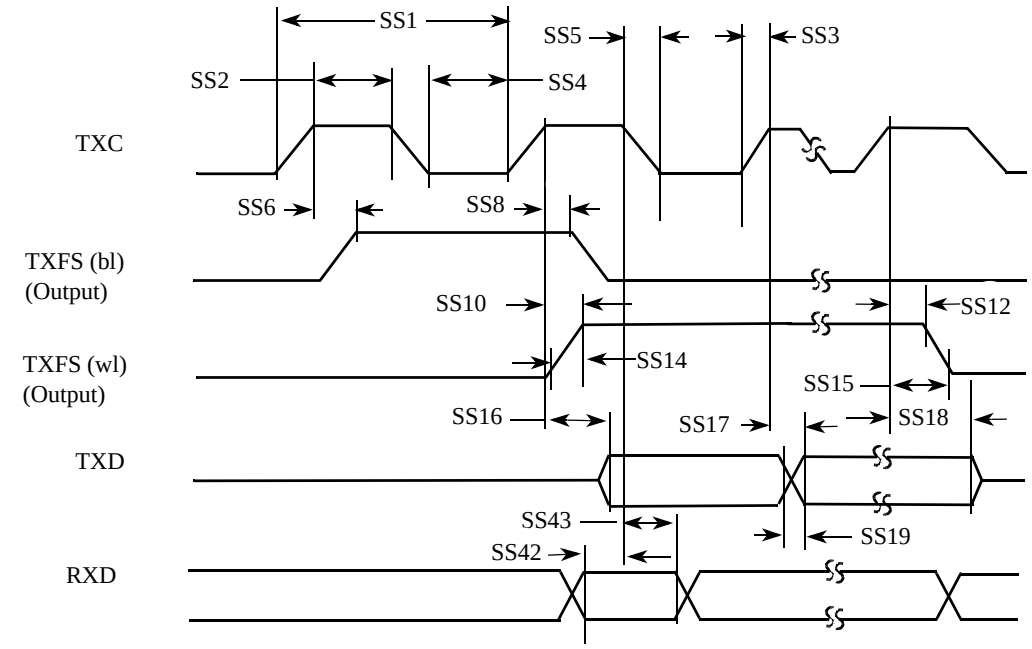
Port	Signal Nomenclature	Type and Access
AUDMUX port 1	SSI 1	Internal
AUDMUX port 2	SSI 2	Internal
AUDMUX port 3	AUD3	External – AUD3 I/O
AUDMUX port 4	AUD4	External – EIM or CSPI1 I/O through IOMUXC
AUDMUX port 5	AUD5	External – EIM or SD1 I/O through IOMUXC
AUDMUX port 6	AUD6	External – EIM or DISP2 through IOMUXC
AUDMUX port 7	SSI 3	Internal

NOTE

- The terms WL and BL used in the timing diagrams and tables refer to Word Length (WL) and Bit Length (BL).
- The SSI timing diagrams use generic signal names wherein the names used in the i.MX 6Dual/6Quad reference manual are channel specific signal names. For example, a channel clock referenced in the IOMUXC chapter as AUD3_TXC appears in the timing diagram as TXC.

4.11.19.1 SSI Transmitter Timing with Internal Clock

Figure 97 depicts the SSI transmitter internal clock timing and Table 82 lists the timing parameters for the SSI transmitter internal clock.



Note: SRXD input in synchronous mode only

Figure 97. SSI Transmitter Internal Clock Timing Diagram

Table 82. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS6	(Tx) CK high to FS (bl) high	—	15.0	ns
SS8	(Tx) CK high to FS (bl) low	—	15.0	ns
SS10	(Tx) CK high to FS (wl) high	—	15.0	ns
SS12	(Tx) CK high to FS (wl) low	—	15.0	ns
SS14	(Tx/Rx) Internal FS rise time	—	6.0	ns
SS15	(Tx/Rx) Internal FS fall time	—	6.0	ns
SS16	(Tx) CK high to STXD valid from high impedance	—	15.0	ns

Table 82. SSI Transmitter Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
SS17	(Tx) CK high to STXD high/low	—	15.0	ns
SS18	(Tx) CK high to STXD high impedance	—	15.0	ns
SS19	STXD rise/fall time	—	6.0	ns
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	10.0	—	ns
SS43	SRXD hold after (Tx) CK falling	0.0	—	ns
SS52	Loading	—	25.0	pF

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.11.19.2 SSI Receiver Timing with Internal Clock

Figure 98 depicts the SSI receiver internal clock timing and Table 83 lists the timing parameters for the receiver timing with the internal clock.

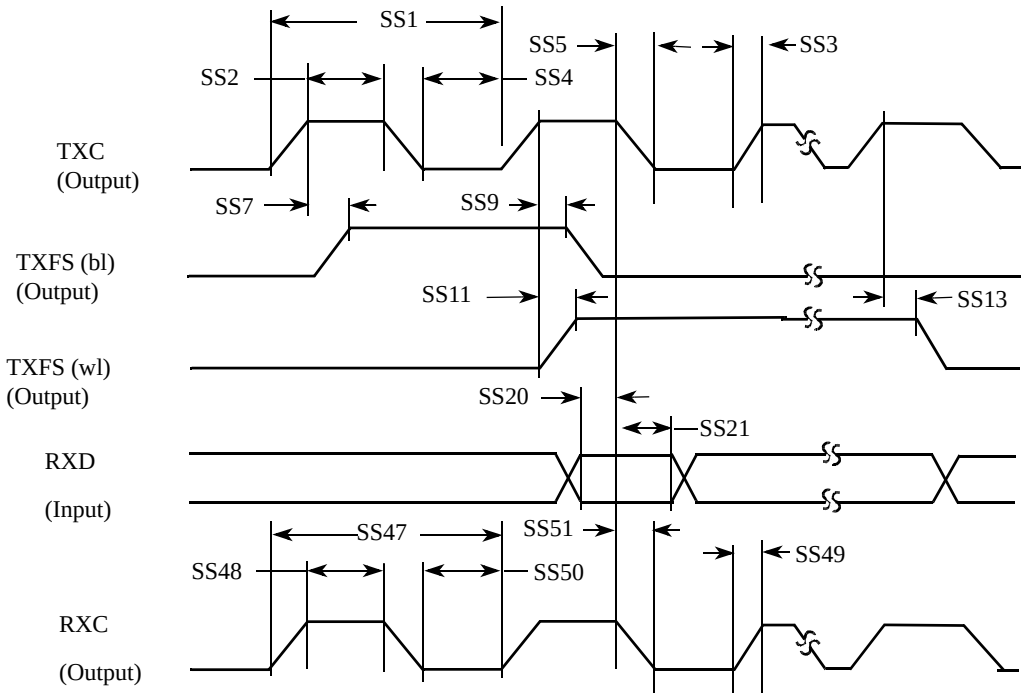


Figure 98. SSI Receiver Internal Clock Timing Diagram

Table 83. SSI Receiver Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	10.0	—	ns
SS21	SRXD hold time after (Rx) CK low	0.0	—	ns
Oversampling Clock Operation				

Table 83. SSI Receiver Timing with Internal Clock (continued)

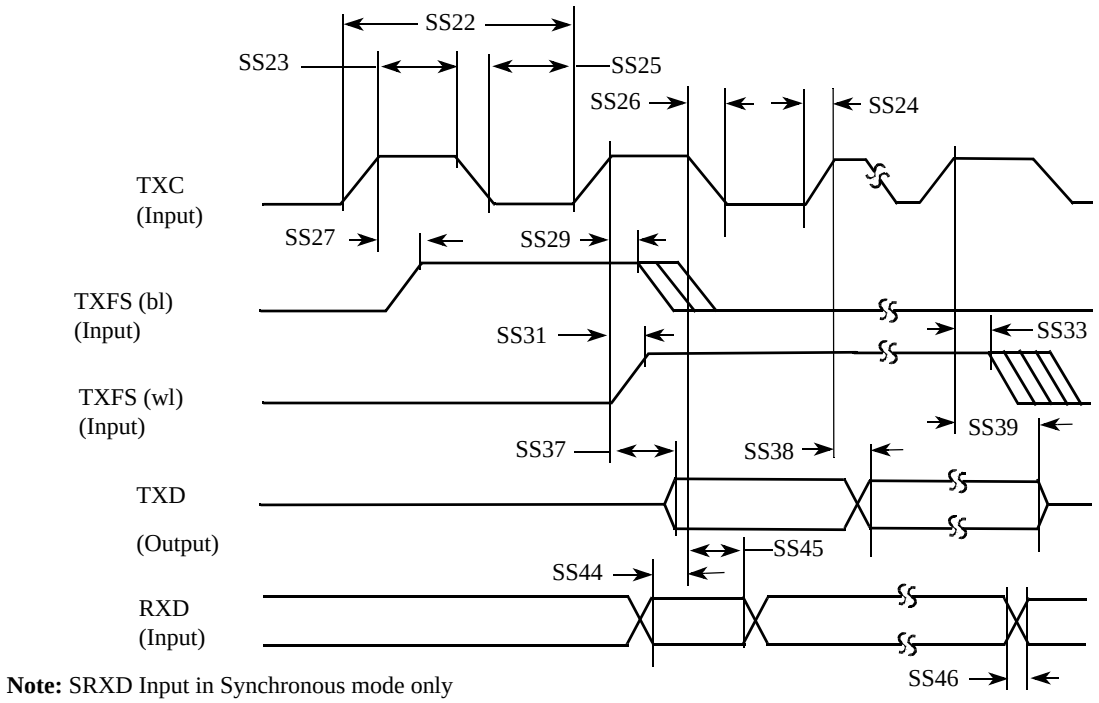
ID	Parameter	Min	Max	Unit
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.11.19.3 SSI Transmitter Timing with External Clock

Figure 99 depicts the SSI transmitter external clock timing and Table 84 lists the timing parameters for the transmitter timing with the external clock.



Note: SRXD Input in Synchronous mode only

Figure 99. SSI Transmitter External Clock Timing Diagram

Table 84. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	–10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	–10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns

Table 84. SSI Transmitter Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.11.19.4 SSI Receiver Timing with External Clock

Figure 100 depicts the SSI receiver external clock timing and Table 85 lists the timing parameters for the receiver timing with the external clock.

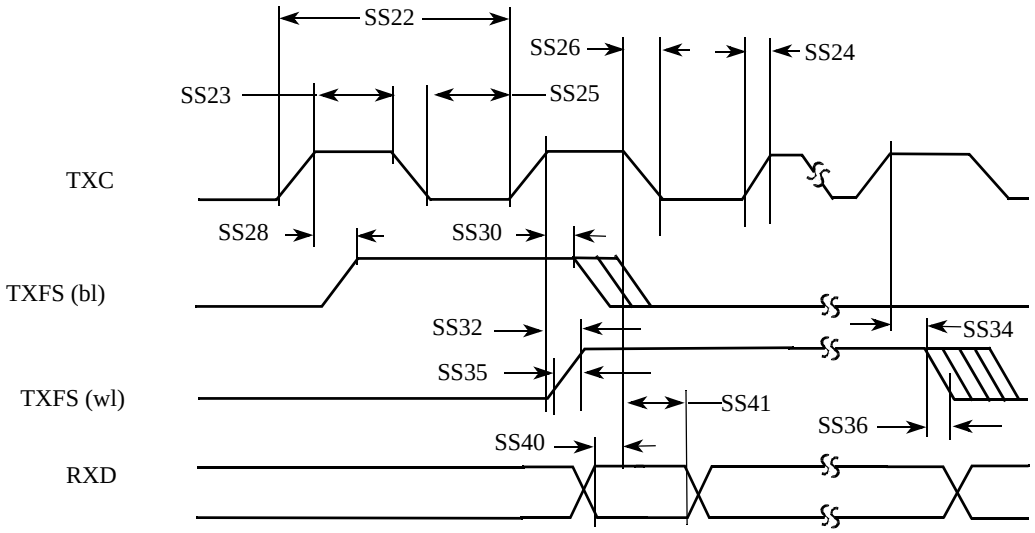


Figure 100. SSI Receiver External Clock Timing Diagram

Table 85. SSI Receiver Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS28	(Rx) CK high to FS (bl) high	–10	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10	—	ns
SS32	(Rx) CK high to FS (wl) high	–10	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10	—	ns
SS41	SRXD hold time after (Rx) CK low	2	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- "Tx" and "Rx" refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.11.20 UART I/O Configuration and Timing Parameters

4.11.20.1 UART RS-232 I/O Configuration in Different Modes

The i.MX 6Dual/6Quad UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0 – DCE mode). Table 86 shows the UART I/O configuration based on the enabled mode.

Table 86. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
RTS	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
CTS	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
DTR	Output	DTR from DTE to DCE	Input	DTR from DTE to DCE
DSR	Input	DSR from DCE to DTE	Output	DSR from DCE to DTE
DCD	Input	DCD from DCE to DTE	Output	DCD from DCE to DTE
RI	Input	RING from DCE to DTE	Output	RING from DCE to DTE
TXD_MUX	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
RXD_MUX	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

4.11.20.2 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.11.20.2.1 UART Transmitter

Figure 101 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 87 lists the UART RS-232 serial mode transmit timing characteristics.

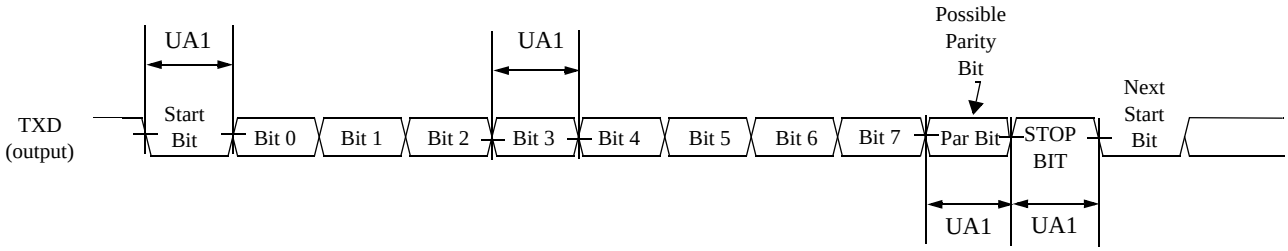


Figure 101. UART RS-232 Serial Mode Transmit Timing Diagram

Table 87. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.11.20.2.2 UART Receiver

Figure 102 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 88 lists serial mode receive timing characteristics.

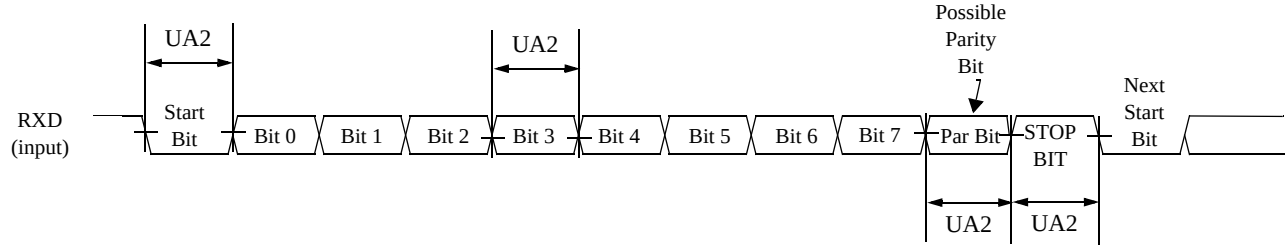


Figure 102. UART RS-232 Serial Mode Receive Timing Diagram

Table 88. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] – $1/(16*F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16*F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16*F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16*F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.11.20.2.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA Mode Transmitter

Figure 103 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 89 lists the transmit timing characteristics.

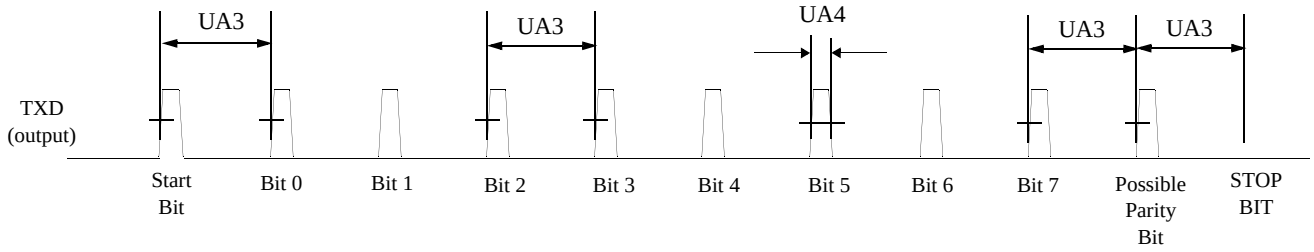


Figure 103. UART IrDA Mode Transmit Timing Diagram

Table 89. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16)*(1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16)*(1/F_{baud\_rate}) + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

UART IrDA Mode Receiver

Figure 104 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 90 lists the receive timing characteristics.

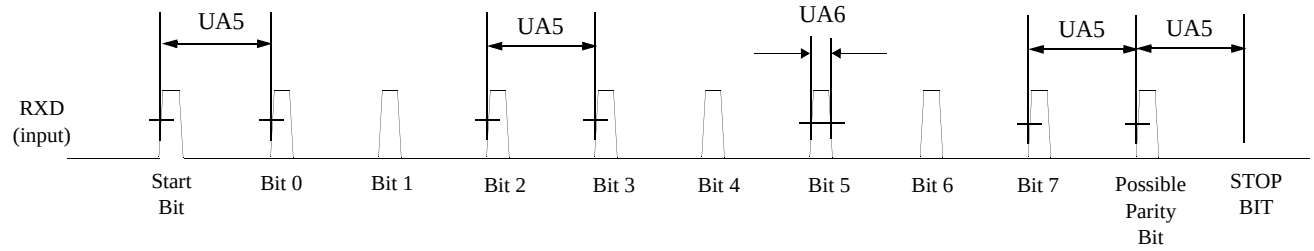


Figure 104. UART IrDA Mode Receive Timing Diagram

Table 90. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] – $1/(16*F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16*F_{baud\_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16)*(1/F_{baud\_rate})$	—

[1] The UART receiver can tolerate 1/(16*F_{baud_rate}) tolerance in each bit. But accumulation tolerance in one frame must not exceed 3/(16*F_{baud_rate}).

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.11.21 USB HSIC Timings

This section describes the electrical information of the USB HSIC port.

NOTE

HSIC is DDR signal, following timing spec is for both rising and falling edge.

4.11.21.1 Transmit Timing

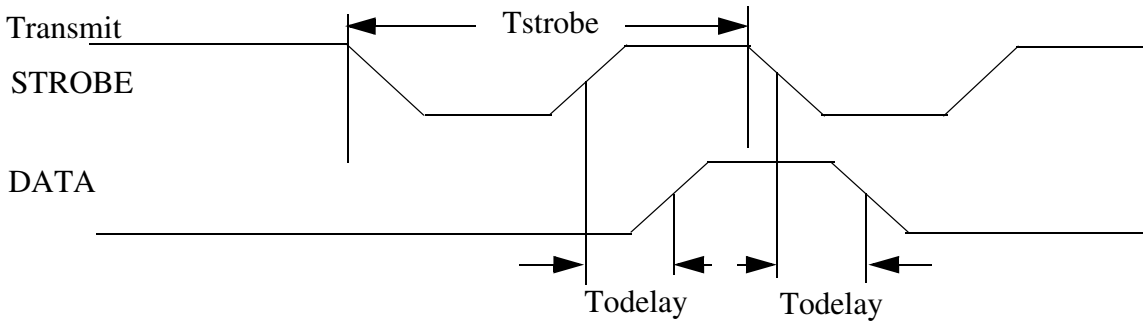


Figure 105. USB HSIC Transmit Waveform

Table 91. USB HSIC Transmit Parameters

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	
Todelay	data output delay time	550	1350	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

4.11.21.2 Receive Timing

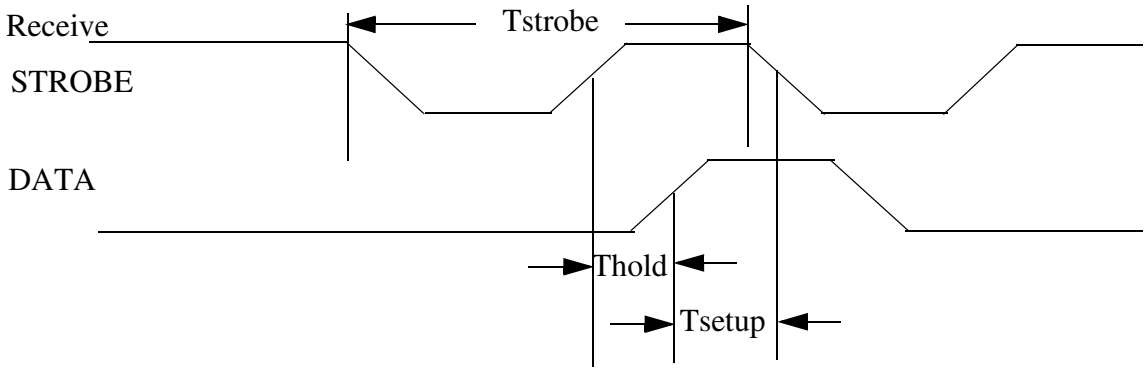


Figure 106. USB HSIC Receive Waveform

Table 92. USB HSIC Receive Parameters

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	
Thold	data hold time	300		ps	Measured at 50% point
Tsetup	data setup time	365		ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

4.11.22 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0

- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Link Power Management Addendum
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 93 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6Dual/6Quad Fuse Map document and the System Boot chapter in i.MX 6Dual/6Quad reference manual.

Table 93. Fuses and Associated Pins Used for Boot

Pin	Direction at Reset	eFuse Name	Details
BOOT_MODE1	Input	Boot Mode Selection	Boot Mode selection
BOOT_MODE0	Input	Boot Mode Selection	Boot Mode Selection

Table 93. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at Reset	eFuse Name	Details
EIM_DA0	Input	BOOT_CFG1[0]	Boot Options, Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.
EIM_DA1	Input	BOOT_CFG1[1]	
EIM_DA2	Input	BOOT_CFG1[2]	
EIM_DA3	Input	BOOT_CFG1[3]	
EIM_DA4	Input	BOOT_CFG1[4]	
EIM_DA5	Input	BOOT_CFG1[5]	
EIM_DA6	Input	BOOT_CFG1[6]	
EIM_DA7	Input	BOOT_CFG1[7]	
EIM_DA8	Input	BOOT_CFG2[0]	
EIM_DA9	Input	BOOT_CFG2[1]	
EIM_DA10	Input	BOOT_CFG2[2]	
EIM_DA11	Input	BOOT_CFG2[3]	
EIM_DA12	Input	BOOT_CFG2[4]	
EIM_DA13	Input	BOOT_CFG2[5]	
EIM_DA14	Input	BOOT_CFG2[6]	
EIM_DA15	Input	BOOT_CFG2[7]	
EIM_A16	Input	BOOT_CFG3[0]	
EIM_A17	Input	BOOT_CFG3[1]	
EIM_A18	Input	BOOT_CFG3[2]	
EIM_A19	Input	BOOT_CFG3[3]	
EIM_A20	Input	BOOT_CFG3[4]	
EIM_A21	Input	BOOT_CFG3[5]	
EIM_A22	Input	BOOT_CFG3[6]	
EIM_A23	Input	BOOT_CFG3[7]	
EIM_A24	Input	BOOT_CFG4[0]	
EIM_WAIT	Input	BOOT_CFG4[1]	
EIM_LBA	Input	BOOT_CFG4[2]	
EIM_EB0	Input	BOOT_CFG4[3]	
EIM_EB1	Input	BOOT_CFG4[4]	
EIM_RW	Input	BOOT_CFG4[5]	
EIM_EB2	Input	BOOT_CFG4[6]	
EIM_EB3	Input	BOOT_CFG4[7]	

5.2 Boot Devices Interfaces Allocation

Table 94 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 94. Interfaces Allocation During Boot

Interface	IP Instance	Allocated Pads During Boot	Comment
SPI	ECSPI-1	EIM_D17, EIM_D18, EIM_D16, EIM_EB2, EIM_D19, EIM_D24, EIM_D25	
SPI	ECSPI-2	CSI0_DAT10, CSI0_DAT9, CSI0_DAT8, CSI0_DAT11, EIM_LBA, EIM_D24, EIM_D25	
SPI	ECSPI-3	DISP0_DAT2, DISP0_DAT1, DISP0_DAT0, DISP0_DAT3, DISP0_DAT4, DISP0_DAT5, DISP0_DAT6	
SPI	ECSPI-4	EIM_D22, EIM_D28, EIM_D21, EIM_D20, EIM_A25, EIM_D24, EIM_D25	
SPI	ECSPI-5	SD1_DAT0, SD1_CMD, SD1_CLK, SD1_DAT1, SD1_DAT2, SD1_DAT3, SD2_DAT3	
EIM	EIM	EIM_DA[15:0], EIM_D[31:16], CSI0_DAT[19:4], CSI0_DATA_EN, CSI0_VSYNC	Only CS0 is supported
NAND Flash	GPMI	NANDF_CLE, NANDF_ALE, NANDF_WP_B, SD4_CMD, SD4_CLK, NANDF_RB0, SD4_DAT0, NANDF_CS0, NANDF_CS1, NANDF_CS2, NANDF_CS3, NANDF_D[7:0]	8 bit Only CS0 is supported
SD/MMC	USDHC-1	SD1_CLK, SD1_CMD,SD1_DAT0, SD1_DAT1, SD1_DAT2, SD1_DAT3, NANDF_D0, NANDF_D1, NANDF_D2, NANDF_D3, KEY_COL1	1, 4, or 8 bit
SD/MMC	USDHC-2	SD2_CLK, SD2_CMD, SD2_DAT0, SD2_DAT1, SD2_DAT2, SD2_DAT3, NANDF_D5, NANDF_D6, NANDF_D7, NANDF_D8, KEY_ROW1	1, 4, or 8 bit
SD/MMC	USDHC-3	SD3_CLK, SD3_CMD, SD3_DAT0, SD3_DAT1, SD3_DAT2, SD3_DAT3, SD3_DAT4, SD3_DAT5, SD3_DAT6, SD3_DAT7, GPIO_18	1, 4, or 8 bit
SD/MMC	USDHC-4	SD4_CLK, SD4_CMD, SD4_DAT0, SD4_DAT1, SD4_DAT2, SD4_DAT3, SD4_DAT4, SD4_DAT5, SD4_DAT6, SD4_DAT7, NANDF_CS1	1, 4, or 8 bit
I2C	I2C-1	EIM_D28, EIM_D21	—
I2C	I2C-2	EIM_D16, EIM_EB2	—
I2C	I2C-3	EIM_D18, EIM_D17	—
SATA	SATA_PHY	SATA_TXM, SATA_TXP, SATA_RXP, SATA_RXM, SATA_REXT, SATA_REFCLKM, SATA_REFCLKP	—
USB	USB-OTG PHY	USB_OTG_DP USB_OTG_DN USB_OTG_VBUS	—

6 Package Information and Contact Assignments

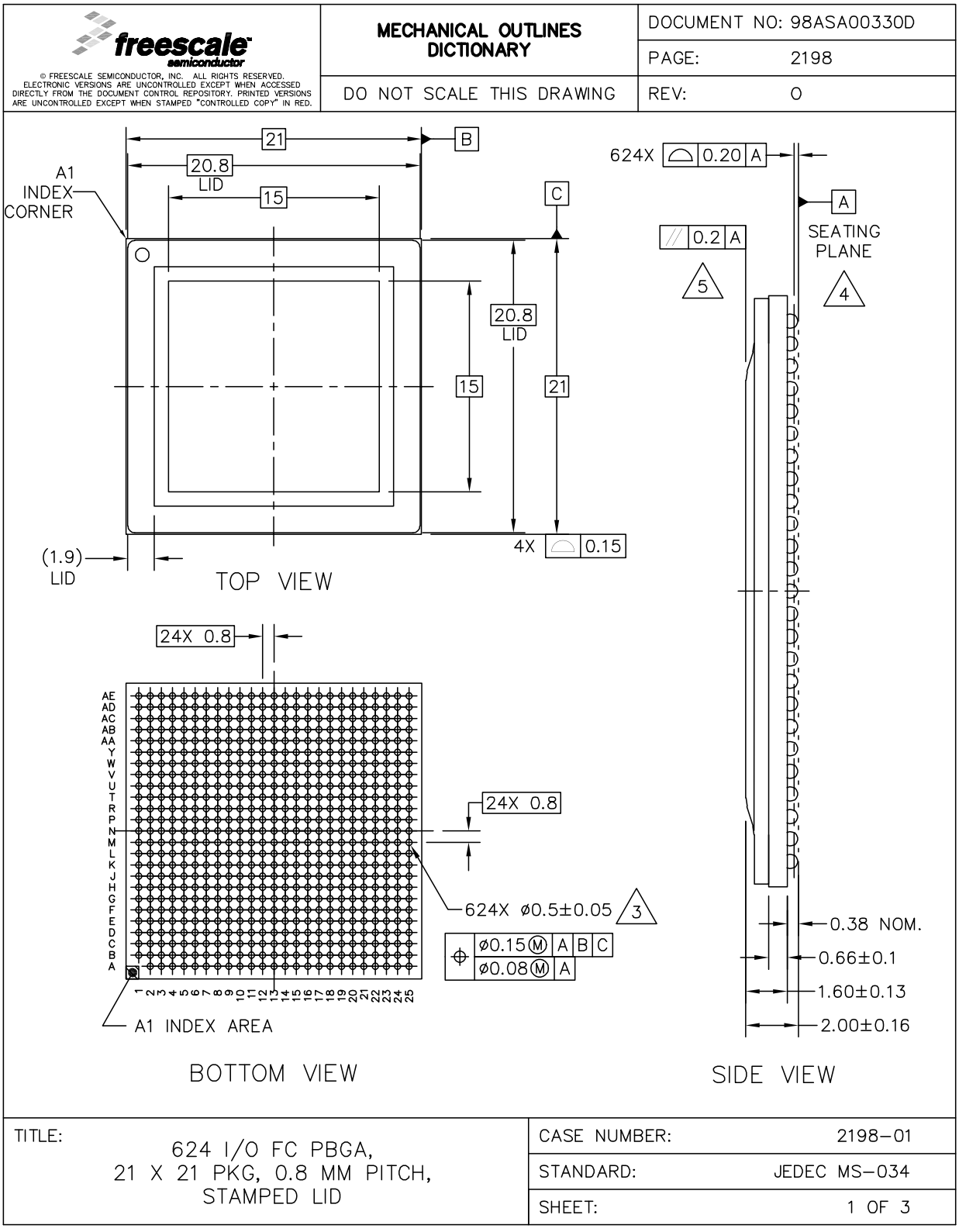
This section includes the contact assignment information and mechanical package drawing.

6.1 21 x 21 mm Package Information

6.1.1 Case FCPBGA, 21 x 21 mm, 0.8 mm Pitch, 25 x 25 Ball Matrix

6.1.1.1 21 x 21 mm Lidded Package

Figure 107 shows the top, bottom, and side views of the 21 × 21 mm lidded package.



freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASA00330D
		PAGE: 2198
	DO NOT SCALE THIS DRAWING	REV: O

NOTES:

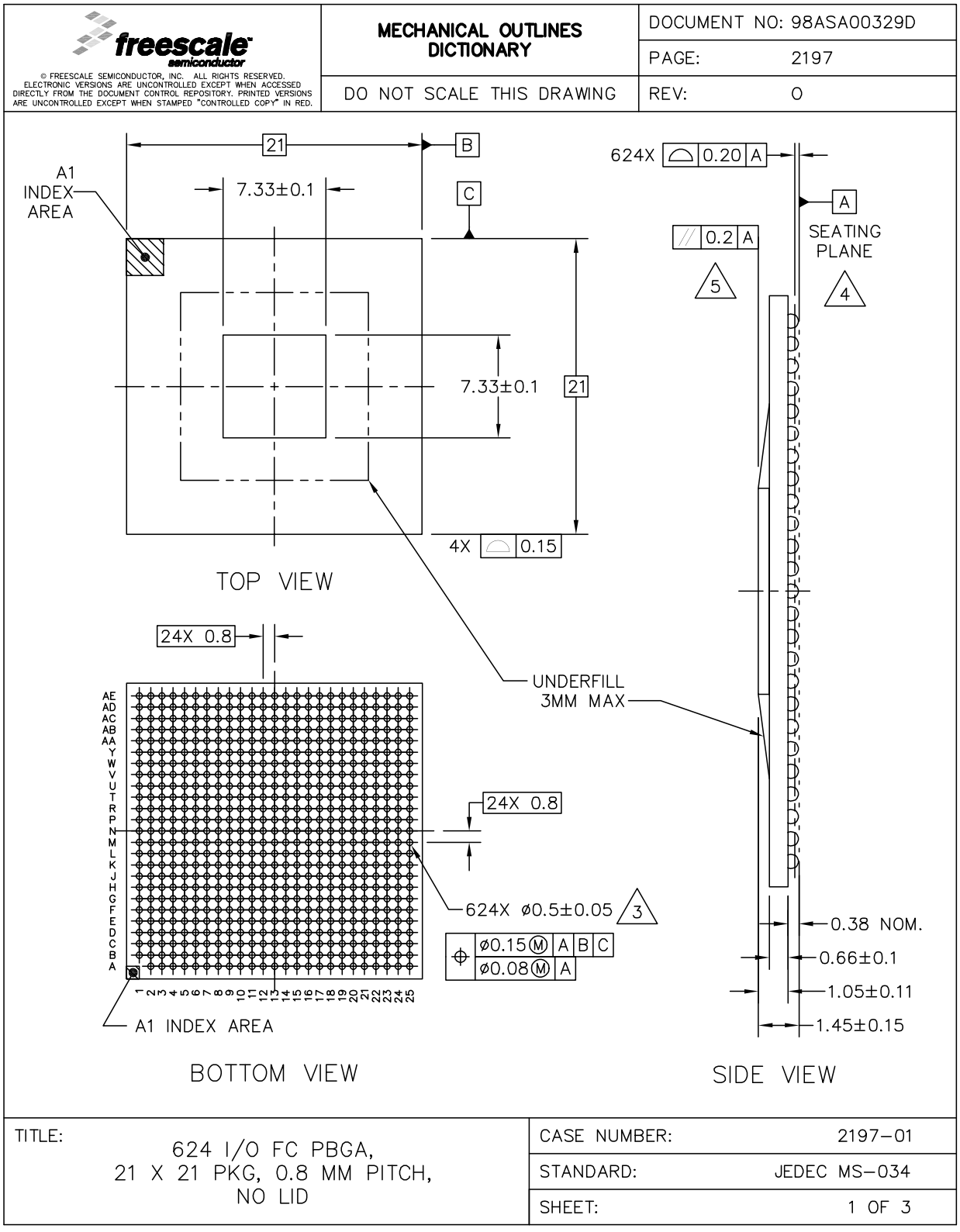
1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TITLE: 624 I/O FC PBGA, 21 X 21 PKG, 0.8 MM PITCH, STAMPED LID	CASE NUMBER:	2198–01
	STANDARD:	JEDEC MS–034
	SHEET:	2

Figure 107. 21 x 21 mm Lidded Package Top, Bottom, and Side Views

6.1.1.2 21 x 21 mm Bare Die Package

Figure 108 shows the top, bottom, and side views of the 21 × 21 mm bare die package.



freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASA00329D
		PAGE: 2197
	DO NOT SCALE THIS DRAWING	REV: O

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TITLE:	CASE NUMBER:	2197–01
624 I/O FC PBGA, 21 X 21 PKG, 0.8 MM PITCH, NO LID	STANDARD:	JEDEC MS–034
	SHEET:	2

Figure 108. 21 x 21 mm Bare Die Package Top, Bottom, and Side Views

6.1.2 21 x 21 mm Ground, Power, Sense, and Reference Contact Assignments

Table 95 shows the device connection list for ground, power, sense, and reference contact signals.

Table 95. 21 x 21 mm Supplies Contact Assignment

Supply Rail Name	Ball(s) Position(s)	Remark
CSI_REXT	D4	
DRAM_VREF	AC2	
DSI_REXT	G4	
FA_ANA	A5	
GND	A13, A25, A4, A8, AA10, AA13, AA16, AA19, AA22, AD4, D3, F8, J15, L10, M15, P15, T15, U8, W17, AA7, AD7, D6, G10, J18, L12, M18, P18, T17, V19, W18, AB24, AE1, D8, G19, J2, L15, M8, P8, T19, V8, W19, AB3, AE25, E5, G3, J8, L18, N10, R12, T8, W10, W3, AD10, B4, E6, H12, K10, L2, N15, R15, U11, W11, W7, AD13, C1, E7, H15, K12, L5, N18, R17, U12, W12, W8, AD16, C10, F5, H18, K15, L8, N8, R8, U15, W13, W9, AD19, C4, F6, H8, K18, M10, P10, T11, U17, W15, Y24, AD22, C6, F7, J12, K8, M12, P12, T12, U19, W16, Y5	
GPANAIO	C8	
HDMI_REF	J1	
HDMI_VP	L7	
HDMI_VPH	M7	
NVCC_CSI	N7	Supply of the Camera Sensor Interface
NVCC_DRAM	R18, T18, U18, V10, V11, V12, V13, V14, V15, V16, V17, V18, V9	Supply of the DDR Interface
NVCC_EIM0	K19	Supply of the EMI Interface
NVCC_EIM1	L19	Supply of the EMI Interface
NVCC_EIM2	M19	Supply of the EMI Interface
NVCC_ENET	R19	Supply of the ENET Interface
NVCC_GPIO	P7	Supply of the GPIO Interface
NVCC_JTAG	J7	Supply of the JTAG Tap Controller Interface
NVCC_LCD	P19	Supply of the LCD Interface
NVCC_LVDS2P5	V7	Supply of the LVDS Display Interface
NVCC_MIPI	K7	Supply of the MIPI Interface
NVCC_NANDF	G15	Supply of the RAW NAND Flash Memories Interface
NVCC_PLL_OUT	E8	

Table 95. 21 x 21 mm Supplies Contact Assignment (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
NVCC_RGMII	G18	Supply of the ENET Interface
NVCC_SD1	G16	Supply of the SD Card Interface
NVCC_SD2	G17	Supply of the SD Card Interface
NVCC_SD3	G14	Supply of the SD Card Interface
PCI_VP	H7	
PCIe_REXT	A2	
PCIE_VPH	G7	PCI PHY Supply
PCIE_VPTX	G8	PCI PHY Supply
SATA_REXT	C14	
SATA_VP	G13	
SATA_VPH	G12	
VDD_CACHE_CAP	N12	Secondary Supply for the L2 Cache Domain (internal regulator output—requires capacitor if internal regulator is use
VDD_FA	B5	
VDD_SNVS_CAP	G9	Secondary Supply for the SNVS (internal regulator output—requires capacitor if internal regulator is use
VDD_SNVS_IN	G11	Primary Supply, for the SNVS Regulator
VDDARM_CAP	H13, J13, K13, L13, M13, N13, P13, R13	Secondary Supply for the ARM0 and ARM1 Cores (internal regulator output—requires capacitor if internal regulator is use
VDDARM_IN	H14, J14, K14, L14, M14, N14, P14, R14	Primary Supply, for the ARM0 and ARM1 Core' Regulator
VDDARM23_CAP	H11, J11, K11, L11, M11, N11, P11, R11	Secondary Supply for the ARM2 and ARM3 Cores (internal regulator output—requires capacitor if internal regulator is use
VDDARM23_IN	K9, L9, M9, N9, P9, R9, T9, U9	Primary Supply, for the ARM2 and ARM3 Core' Regulator
VDDHIGH_CAP	H10, J10	Secondary Supply for the 2.5 V domain (internal regulator output—requires capacitor if internal regulator is use
VDDHIGH_IN	H9, J9	Primary Supply, for the 2.5 V Regulator

Table 95. 21 x 21 mm Supplies Contact Assignment (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
VDDPU_CAP	H17, J17, K17, L17, M17, N17, P17	Secondary Supply for the VPU and GPU's (internal regulator output—requires capacitor if internal regulator is use
VDDSOC_CAP	R10, T10, T13, T14, U10, U13, U14	Secondary Supply for the SOC and PU (internal regulator output—requires capacitor if internal regulator is use
VDDSOC_IN	H16, J16, K16, L16, M16, N16, P16, R16, T16, U16	Primary Supply, for the SOC and PU Regulators
VDDUSB_CAP	F9	Secondary Supply for the 3 V Domain (USBPHY, MLPBPHY, eFuse) (internal regulator output—requires capacitor if internal regulator is use
ZQPAD	AE17	

Table 96 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

Table 96. 21 x 21 mm Functional Contact Assignments

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
BOOT_MODE0	C12	VDD_SNVS_IN	GPIO	ALT0	src_BOOT_MODE[0]	Input	PD (100K)
BOOT_MODE1	F12	VDD_SNVS_IN	GPIO	ALT0	src_BOOT_MODE[1]	Input	PD (100K)
CLK1_N	C7	ANATOP			CLK1_N	—	—
CLK1_P	D7	ANATOP			CLK1_P	—	—
CLK2_N	C5	ANATOP			CLK2_N	—	—
CLK2_P	D5	ANATOP			CLK2_P	—	—
CSI_CLK0M	F4	NVCC_MIPI			CSI_CLK0M	—	—
CSI_CLK0P	F3	NVCC_MIPI			CSI_CLK0P	—	—
CSI_D0M	E4	NVCC_MIPI			CSI_D0M	—	—
CSI_D0P	E3	NVCC_MIPI			CSI_D0P	—	—
CSI_D1M	D1	NVCC_MIPI			CSI_D1M	—	—
CSI_D1P	D2	NVCC_MIPI			CSI_D1P	—	—
CSI_D2M	E1	NVCC_MIPI			CSI_D2M	—	—
CSI_D2P	E2	NVCC_MIPI			CSI_D2P	—	—
CSI_D3M	F2	NVCC_MIPI			CSI_D3M	—	—

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
CSI_D3P	F1	NVCC_MIPI			CSI_D3P	—	—
CSI0_DAT10	M1	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[28]	Input	PU (100K)
CSI0_DAT11	M3	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[29]	Input	PU (100K)
CSI0_DAT12	M2	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[30]	Input	PU (100K)
CSI0_DAT13	L1	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[31]	Input	PU (100K)
CSI0_DAT14	M4	NVCC_CSI	GPIO	ALT5	gpio6_GPIO[0]	Input	PU (100K)
CSI0_DAT15	M5	NVCC_CSI	GPIO	ALT5	gpio6_GPIO[1]	Input	PU (100K)
CSI0_DAT16	L4	NVCC_CSI	GPIO	ALT5	gpio6_GPIO[2]	Input	PU (100K)
CSI0_DAT17	L3	NVCC_CSI	GPIO	ALT5	gpio6_GPIO[3]	Input	PU (100K)
CSI0_DAT18	M6	NVCC_CSI	GPIO	ALT5	gpio6_GPIO[4]	Input	PU (100K)
CSI0_DAT19	L6	NVCC_CSI	GPIO	ALT5	gpio6_GPIO[5]	Input	PU (100K)
CSI0_DAT4	N1	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[22]	Input	PU (100K)
CSI0_DAT5	P2	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[23]	Input	PU (100K)
CSI0_DAT6	N4	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[24]	Input	PU (100K)
CSI0_DAT7	N3	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[25]	Input	PU (100K)
CSI0_DAT8	N6	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[26]	Input	PU (100K)
CSI0_DAT9	N5	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[27]	Input	PU (100K)
CSI0_DATA_EN	P3	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[20]	Input	PU (100K)
CSI0_MCLK	P4	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[19]	Input	PU (100K)
CSI0_PIXCLK	P1	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[18]	Input	PU (100K)
CSI0_VSYNC	N2	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[21]	Input	PU (100K)
DI0_DISP_CLK	N19	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[16]	Input	PU (100K)
DI0_PIN15	N21	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[17]	Input	PU (100K)
DI0_PIN2	N25	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[18]	Input	PU (100K)
DI0_PIN3	N20	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[19]	Input	PU (100K)
DI0_PIN4	P25	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[20]	Input	PU (100K)
DISP0_DAT0	P24	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[21]	Input	PU (100K)
DISP0_DAT1	P22	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[22]	Input	PU (100K)
DISP0_DAT10	R21	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[31]	Input	PU (100K)
DISP0_DAT11	T23	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[5]	Input	PU (100K)

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
DISP0_DAT12	T24	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[6]	Input	PU (100K)
DISP0_DAT13	R20	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[7]	Input	PU (100K)
DISP0_DAT14	U25	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[8]	Input	PU (100K)
DISP0_DAT15	T22	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[9]	Input	PU (100K)
DISP0_DAT16	T21	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[10]	Input	PU (100K)
DISP0_DAT17	U24	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[11]	Input	PU (100K)
DISP0_DAT18	V25	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[12]	Input	PU (100K)
DISP0_DAT19	U23	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[13]	Input	PU (100K)
DISP0_DAT2	P23	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[23]	Input	PU (100K)
DISP0_DAT20	U22	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[14]	Input	PU (100K)
DISP0_DAT21	T20	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[15]	Input	PU (100K)
DISP0_DAT22	V24	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[16]	Input	PU (100K)
DISP0_DAT23	W24	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[17]	Input	PU (100K)
DISP0_DAT3	P21	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[24]	Input	PU (100K)
DISP0_DAT4	P20	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[25]	Input	PU (100K)
DISP0_DAT5	R25	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[26]	Input	PU (100K)
DISP0_DAT6	R23	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[27]	Input	PU (100K)
DISP0_DAT7	R24	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[28]	Input	PU (100K)
DISP0_DAT8	R22	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[29]	Input	PU (100K)
DISP0_DAT9	T25	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[30]	Input	PU (100K)
DRAM_A0	AC14	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[0]	Output	0
DRAM_A1	AB14	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[1]	Output	0
DRAM_A10	AA15	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[10]	Output	0
DRAM_A11	AC12	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[11]	Output	0
DRAM_A12	AD12	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[12]	Output	0
DRAM_A13	AC17	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[13]	Output	0
DRAM_A14	AA12	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[14]	Output	0
DRAM_A15	Y12	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[15]	Output	0
DRAM_A2	AA14	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[2]	Output	0
DRAM_A3	Y14	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[3]	Output	0

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
DRAM_A4	W14	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[4]	Output	0
DRAM_A5	AE13	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[5]	Output	0
DRAM_A6	AC13	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[6]	Output	0
DRAM_A7	Y13	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[7]	Output	0
DRAM_A8	AB13	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[8]	Output	0
DRAM_A9	AE12	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[9]	Output	0
DRAM_CAS	AE16	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_CAS	Output	0
DRAM_CS0	Y16	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_CS[0]	Output	0
DRAM_CS1	AD17	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_CS[1]	Output	0
DRAM_D0	AD2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[0]	Input	PU (100K)
DRAM_D1	AE2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[1]	Input	PU (100K)
DRAM_D10	AA6	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[10]	Input	PU (100K)
DRAM_D11	AE7	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[11]	Input	PU (100K)
DRAM_D12	AB5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[12]	Input	PU (100K)
DRAM_D13	AC5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[13]	Input	PU (100K)
DRAM_D14	AB6	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[14]	Input	PU (100K)
DRAM_D15	AC7	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[15]	Input	PU (100K)
DRAM_D16	AB7	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[16]	Input	PU (100K)
DRAM_D17	AA8	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[17]	Input	PU (100K)
DRAM_D18	AB9	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[18]	Input	PU (100K)
DRAM_D19	Y9	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[19]	Input	PU (100K)
DRAM_D2	AC4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[2]	Input	PU (100K)
DRAM_D20	Y7	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[20]	Input	PU (100K)
DRAM_D21	Y8	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[21]	Input	PU (100K)
DRAM_D22	AC8	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[22]	Input	PU (100K)
DRAM_D23	AA9	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[23]	Input	PU (100K)
DRAM_D24	AE9	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[24]	Input	PU (100K)
DRAM_D25	Y10	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[25]	Input	PU (100K)
DRAM_D26	AE11	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[26]	Input	PU (100K)
DRAM_D27	AB11	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[27]	Input	PU (100K)

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
DRAM_D28	AC9	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[28]	Input	PU (100K)
DRAM_D29	AD9	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[29]	Input	PU (100K)
DRAM_D3	AA5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[3]	Input	PU (100K)
DRAM_D30	AD11	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[30]	Input	PU (100K)
DRAM_D31	AC11	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[31]	Input	PU (100K)
DRAM_D32	AA17	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[32]	Input	PU (100K)
DRAM_D33	AA18	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[33]	Input	PU (100K)
DRAM_D34	AC18	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[34]	Input	PU (100K)
DRAM_D35	AE19	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[35]	Input	PU (100K)
DRAM_D36	Y17	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[36]	Input	PU (100K)
DRAM_D37	Y18	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[37]	Input	PU (100K)
DRAM_D38	AB19	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[38]	Input	PU (100K)
DRAM_D39	AC19	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[39]	Input	PU (100K)
DRAM_D4	AC1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[4]	Input	PU (100K)
DRAM_D40	Y19	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[40]	Input	PU (100K)
DRAM_D41	AB20	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[41]	Input	PU (100K)
DRAM_D42	AB21	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[42]	Input	PU (100K)
DRAM_D43	AD21	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[43]	Input	PU (100K)
DRAM_D44	Y20	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[44]	Input	PU (100K)
DRAM_D45	AA20	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[45]	Input	PU (100K)
DRAM_D46	AE21	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[46]	Input	PU (100K)
DRAM_D47	AC21	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[47]	Input	PU (100K)
DRAM_D48	AC22	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[48]	Input	PU (100K)
DRAM_D49	AE22	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[49]	Input	PU (100K)
DRAM_D5	AD1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[5]	Input	PU (100K)
DRAM_D50	AE24	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[50]	Input	PU (100K)
DRAM_D51	AC24	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[51]	Input	PU (100K)
DRAM_D52	AB22	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[52]	Input	PU (100K)
DRAM_D53	AC23	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[53]	Input	PU (100K)
DRAM_D54	AD25	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[54]	Input	PU (100K)

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
DRAM_D55	AC25	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[55]	Input	PU (100K)
DRAM_D56	AB25	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[56]	Input	PU (100K)
DRAM_D57	AA21	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[57]	Input	PU (100K)
DRAM_D58	Y25	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[58]	Input	PU (100K)
DRAM_D59	Y22	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[59]	Input	PU (100K)
DRAM_D6	AB4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[6]	Input	PU (100K)
DRAM_D60	AB23	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[60]	Input	PU (100K)
DRAM_D61	AA23	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[61]	Input	PU (100K)
DRAM_D62	Y23	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[62]	Input	PU (100K)
DRAM_D63	W25	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[63]	Input	PU (100K)
DRAM_D7	AE4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[7]	Input	PU (100K)
DRAM_D8	AD5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[8]	Input	PU (100K)
DRAM_D9	AE5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[9]	Input	PU (100K)
DRAM_DQM0	AC3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[0]	Output	0
DRAM_DQM1	AC6	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[1]	Output	0
DRAM_DQM2	AB8	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[2]	Output	0
DRAM_DQM3	AE10	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[3]	Output	0
DRAM_DQM4	AB18	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[4]	Output	0
DRAM_DQM5	AC20	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[5]	Output	0
DRAM_DQM6	AD24	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[6]	Output	0
DRAM_DQM7	Y21	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[7]	Output	0
DRAM_RAS	AB15	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_RAS	Output	0
DRAM_RESET	Y6	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_RESET	Output	0
DRAM_SDBA0	AC15	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDBA[0]	Output	0
DRAM_SDBA1	Y15	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDBA[1]	Output	0
DRAM_SDBA2	AB12	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDBA[2]	Output	0
DRAM_SDCKE0	Y11	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDCKE[0]	Output	0
DRAM_SDCKE1	AA11	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDCKE[1]	Output	0
DRAM_SDCLK_0	AD15	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDCLK0	Input	Hi-Z
DRAM_SDCLK_0_B	AE15	NVCC_DRAM	DDRCLK		DRAM_SDCLK_0_B	—	—

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
DRAM_SDCLK_1	AD14	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDCLK1	Input	Hi-Z
DRAM_SDCLK_1_B	AE14	NVCC_DRAM	DDRCLK		DRAM_SDCLK_1_B	—	—
DRAM_SDODT0	AC16	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_ODT[0]	Output	0
DRAM_SDODT1	AB17	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_ODT[1]	Output	0
DRAM_SDQS0	AE3	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[0]	Input	Hi-Z
DRAM_SDQS0_B	AD3	NVCC_DRAM	DDRCLK		DRAM_SDQS0_B	—	—
DRAM_SDQS1	AD6	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[1]	Input	Hi-Z
DRAM_SDQS1_B	AE6	NVCC_DRAM	DDRCLK		DRAM_SDQS1_B	—	—
DRAM_SDQS2	AD8	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[2]	Input	Hi-Z
DRAM_SDQS2_B	AE8	NVCC_DRAM	DDRCLK		DRAM_SDQS2_B	—	—
DRAM_SDQS3	AC10	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[3]	Input	Hi-Z
DRAM_SDQS3_B	AB10	NVCC_DRAM	DDRCLK		DRAM_SDQS3_B	—	—
DRAM_SDQS4	AD18	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[4]	Input	Hi-Z
DRAM_SDQS4_B	AE18	NVCC_DRAM	DDRCLK		DRAM_SDQS4_B	—	—
DRAM_SDQS5	AD20	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[5]	Input	Hi-Z
DRAM_SDQS5_B	AE20	NVCC_DRAM	DDRCLK		DRAM_SDQS5_B	—	—
DRAM_SDQS6	AD23	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[6]	Input	Hi-Z
DRAM_SDQS6_B	AE23	NVCC_DRAM	DDRCLK		DRAM_SDQS6_B	—	—
DRAM_SDQS7	AA25	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[7]	Input	Hi-Z
DRAM_SDQS7_B	AA24	NVCC_DRAM	DDRCLK		DRAM_SDQS7_B	—	—
DRAM_SDWE	AB16	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDWE	Output	0
DSI_CLK0M	H3	NVCC_MIPI			DSI_CLK0M	—	—
DSI_CLK0P	H4	NVCC_MIPI			DSI_CLK0P	—	—
DSI_D0M	G2	NVCC_MIPI			DSI_D0M	—	—
DSI_D0P	G1	NVCC_MIPI			DSI_D0P	—	—
DSI_D1M	H2	NVCC_MIPI			DSI_D1M	—	—
DSI_D1P	H1	NVCC_MIPI			DSI_D1P	—	—
EIM_A16	H25	NVCC_EIM1	GPIO	ALT0	weim_WEIM_A[16]	Output	0
EIM_A17	G24	NVCC_EIM1	GPIO	ALT0	weim_WEIM_A[17]	Output	0
EIM_A18	J22	NVCC_EIM1	GPIO	ALT0	weim_WEIM_A[18]	Output	0

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
EIM_A19	G25	NVCC_EIM1	GPIO	ALT0	weim_WEIM_A[19]	Output	0
EIM_A20	H22	NVCC_EIM1	GPIO	ALT0	weim_WEIM_A[20]	Output	0
EIM_A21	H23	NVCC_EIM1	GPIO	ALT0	weim_WEIM_A[21]	Output	0
EIM_A22	F24	NVCC_EIM1	GPIO	ALT0	weim_WEIM_A[22]	Output	0
EIM_A23	J21	NVCC_EIM1	GPIO	ALT0	weim_WEIM_A[23]	Output	0
EIM_A24	F25	NVCC_EIM1	GPIO	ALT0	weim_WEIM_A[24]	Output	0
EIM_A25	H19	NVCC_EIM0	GPIO	ALT0	weim_WEIM_A[25]	Output	0
EIM_BCLK	N22	NVCC_EIM2	GPIO	ALT0	weim_WEIM_BCLK	Output	0
EIM_CS0	H24	NVCC_EIM1	GPIO	ALT0	weim_WEIM_CS[0]	Output	1
EIM_CS1	J23	NVCC_EIM1	GPIO	ALT0	weim_WEIM_CS[1]	Output	1
EIM_D16	C25	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[16]	Input	PU (100K)
EIM_D17	F21	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[17]	Input	PU (100K)
EIM_D18	D24	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[18]	Input	PU (100K)
EIM_D19	G21	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[19]	Input	PU (100K)
EIM_D20	G20	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[20]	Input	PU (100K)
EIM_D21	H20	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[21]	Input	PU (100K)
EIM_D22	E23	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[22]	Input	PD (100K)
EIM_D23	D25	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[23]	Input	PU (100K)
EIM_D24	F22	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[24]	Input	PU (100K)
EIM_D25	G22	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[25]	Input	PU (100K)
EIM_D26	E24	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[26]	Input	PU (100K)
EIM_D27	E25	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[27]	Input	PU (100K)
EIM_D28	G23	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[28]	Input	PU (100K)
EIM_D29	J19	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[29]	Input	PU (100K)
EIM_D30	J20	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[30]	Input	PU (100K)
EIM_D31	H21	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[31]	Input	PD (100K)
EIM_DA0	L20	NVCC_EIM2	GPIO	ALT0	weim_WEIM_DA_A[0]	Input	PU (100K)
EIM_DA1	J25	NVCC_EIM2	GPIO	ALT0	weim_WEIM_DA_A[1]	Input	PU (100K)
EIM_DA10	M22	NVCC_EIM2	GPIO	ALT0	weim_WEIM_DA_A[10]	Input	PU (100K)
EIM_DA11	M20	NVCC_EIM2	GPIO	ALT0	weim_WEIM_DA_A[11]	Input	PU (100K)

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
EIM_DA12	M24	NVCC_EIM2	GPIO	ALT0	weim_WEIM_DA_A[12]	Input	PU (100K)
EIM_DA13	M23	NVCC_EIM2	GPIO	ALT0	weim_WEIM_DA_A[13]	Input	PU (100K)
EIM_DA14	N23	NVCC_EIM2	GPIO	ALT0	weim_WEIM_DA_A[14]	Input	PU (100K)
EIM_DA15	N24	NVCC_EIM2	GPIO	ALT0	weim_WEIM_DA_A[15]	Input	PU (100K)
EIM_DA2	L21	NVCC_EIM2	GPIO	ALT0	weim_WEIM_DA_A[2]	Input	PU (100K)
EIM_DA3	K24	NVCC_EIM2	GPIO	ALT0	weim_WEIM_DA_A[3]	Input	PU (100K)
EIM_DA4	L22	NVCC_EIM2	GPIO	ALT0	weim_WEIM_DA_A[4]	Input	PU (100K)
EIM_DA5	L23	NVCC_EIM2	GPIO	ALT0	weim_WEIM_DA_A[5]	Input	PU (100K)
EIM_DA6	K25	NVCC_EIM2	GPIO	ALT0	weim_WEIM_DA_A[6]	Input	PU (100K)
EIM_DA7	L25	NVCC_EIM2	GPIO	ALT0	weim_WEIM_DA_A[7]	Input	PU (100K)
EIM_DA8	L24	NVCC_EIM2	GPIO	ALT0	weim_WEIM_DA_A[8]	Input	PU (100K)
EIM_DA9	M21	NVCC_EIM2	GPIO	ALT0	weim_WEIM_DA_A[9]	Input	PU (100K)
EIM_EB0	K21	NVCC_EIM2	GPIO	ALT0	weim_WEIM_EB[0]	Output	1
EIM_EB1	K23	NVCC_EIM2	GPIO	ALT0	weim_WEIM_EB[1]	Output	1
EIM_EB2	E22	NVCC_EIM0	GPIO	ALT5	gpio2_GPIO[30]	Input	PU (100K)
EIM_EB3	F23	NVCC_EIM0	GPIO	ALT5	gpio2_GPIO[31]	Input	PU (100K)
EIM_LBA	K22	NVCC_EIM1	GPIO	ALT0	weim_WEIM_LBA	Output	1
EIM_OE	J24	NVCC_EIM1	GPIO	ALT0	weim_WEIM_OE	Output	1
EIM_RW	K20	NVCC_EIM1	GPIO	ALT0	weim_WEIM_RW	Output	1
EIM_WAIT	M25	NVCC_EIM2	GPIO	ALT0	weim_WEIM_WAIT	Input	PU (100K)
ENET_CRS_DV	U21	NVCC_ENET	GPIO	ALT5	gpio1_GPIO[25]	Input	PU (100K)
ENET_MDC	V20	NVCC_ENET	GPIO	ALT5	gpio1_GPIO[31]	Input	PU (100K)
ENET_MDIO	V23	NVCC_ENET	GPIO	ALT5	gpio1_GPIO[22]	Input	PU (100K)
ENET_REF_CLK	V22	NVCC_ENET	GPIO	ALT5	gpio1_GPIO[23]	Input	PU (100K)
ENET_RX_ER	W23	NVCC_ENET	GPIO	ALT5	gpio1_GPIO[24]	Input	PU (100K)
ENET_RXD0	W21	NVCC_ENET	GPIO	ALT5	gpio1_GPIO[27]	Input	PU (100K)
ENET_RXD1	W22	NVCC_ENET	GPIO	ALT5	gpio1_GPIO[26]	Input	PU (100K)
ENET_TX_EN	V21	NVCC_ENET	GPIO	ALT5	gpio1_GPIO[28]	Input	PU (100K)
ENET_TXD0	U20	NVCC_ENET	GPIO	ALT5	gpio1_GPIO[30]	Input	PU (100K)
ENET_TXD1	W20	NVCC_ENET	GPIO	ALT5	gpio1_GPIO[29]	Input	PU (100K)

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
GPIO_0	T5	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[0]	Input	PD (100K)
GPIO_1	T4	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[1]	Input	PD (100K)
GPIO_16	R2	NVCC_GPIO	GPIO	ALT5	gpio7_GPIO[11]	Input	PU (100K)
GPIO_17	R1	NVCC_GPIO	GPIO	ALT5	gpio7_GPIO[12]	Input	PU (100K)
GPIO_18	P6	NVCC_GPIO	GPIO	ALT5	gpio7_GPIO[13]	Input	PU (100K)
GPIO_19	P5	NVCC_GPIO	GPIO	ALT5	gpio7_GPIO[5]	Input	PU (100K)
GPIO_2	T1	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[2]	Input	PU (100K)
GPIO_3	R7	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[3]	Input	PU (100K)
GPIO_4	R6	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[4]	Input	PU (100K)
GPIO_5	R4	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[5]	Input	PU (100K)
GPIO_6	T3	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[6]	Input	PU (100K)
GPIO_7	R3	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[7]	Input	PU (100K)
GPIO_8	R5	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[8]	Input	PU (100K)
GPIO_9	T2	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[9]	Input	PU (100K)
HDMI_CLKM	J5	HDMI			HDMI_CLKM	—	—
HDMI_CLKP	J6	HDMI			HDMI_CLKP	—	—
HDMI_D0M	K5	HDMI			HDMI_D0M	—	—
HDMI_D0P	K6	HDMI			HDMI_D0P	—	—
HDMI_D1M	J3	HDMI			HDMI_D1M	—	—
HDMI_D1P	J4	HDMI			HDMI_D1P	—	—
HDMI_D2M	K3	HDMI			HDMI_D2M	—	—
HDMI_D2P	K4	HDMI			HDMI_D2P	—	—
HDMI_DDCCEC	K2	HDMI			HDMI_DDCCEC	—	—
HDMI_HPD	K1	HDMI			HDMI_HPD	—	—
JTAG_MOD	H6	NVCC_JTAG	GPIO	ALT0	sjc_MOD	Input	PU (100K)
JTAG_TCK	H5	NVCC_JTAG	GPIO	ALT0	sjc_TCK	Input	PU (47K)
JTAG_TDI	G5	NVCC_JTAG	GPIO	ALT0	sjc_TDI	Input	PU (47K)
JTAG_TDO	G6	NVCC_JTAG	GPIO	ALT0	sjc_TDO	Output	Keeper
JTAG_TMS	C3	NVCC_JTAG	GPIO	ALT0	sjc_TMS	Input	PU (47K)
JTAG_TRSTB	C2	NVCC_JTAG	GPIO	ALT0	sjc_TRSTB	Input	PU (47K)

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
KEY_COL0	W5	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[6]	Input	PU (100K)
KEY_COL1	U7	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[8]	Input	PU (100K)
KEY_COL2	W6	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[10]	Input	PU (100K)
KEY_COL3	U5	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[12]	Input	PU (100K)
KEY_COL4	T6	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[14]	Input	PU (100K)
KEY_ROW0	V6	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[7]	Input	PU (100K)
KEY_ROW1	U6	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[9]	Input	PU (100K)
KEY_ROW2	W4	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[11]	Input	PU (100K)
KEY_ROW3	T7	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[13]	Input	PU (100K)
KEY_ROW4	V5	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[15]	Input	PD (100K)
LVDS0_CLK_N	V4	NVCC_LVDS	LVDS		LVDS0_CLK_N	—	—
LVDS0_CLK_P	V3	NVCC_LVDS	LVDS	ALT0	ldb_LVDS0_CLK	Input	Keeper
LVDS0_TX0_N	U2	NVCC_LVDS	LVDS		LVDS0_TX0_N	—	—
LVDS0_TX0_P	U1	NVCC_LVDS	LVDS	ALT0	ldb_LVDS0_TX0	Input	Keeper
LVDS0_TX1_N	U4	NVCC_LVDS	LVDS		LVDS0_TX1_N	—	—
LVDS0_TX1_P	U3	NVCC_LVDS	LVDS	ALT0	ldb_LVDS0_TX1	Input	Keeper
LVDS0_TX2_N	V2	NVCC_LVDS	LVDS		LVDS0_TX2_N	—	—
LVDS0_TX2_P	V1	NVCC_LVDS	LVDS	ALT0	ldb_LVDS0_TX2	Input	Keeper
LVDS0_TX3_N	W2	NVCC_LVDS	LVDS		LVDS0_TX3_N	—	—
LVDS0_TX3_P	W1	NVCC_LVDS	LVDS	ALT0	ldb_LVDS0_TX3	Input	Keeper
LVDS1_CLK_N	Y3	NVCC_LVDS	LVDS		LVDS1_CLK_N	—	—
LVDS1_CLK_P	Y4	NVCC_LVDS	LVDS	ALT0	ldb_LVDS1_CLK	Input	Keeper
LVDS1_TX0_N	Y1	NVCC_LVDS	LVDS		LVDS1_TX0_N	—	—
LVDS1_TX0_P	Y2	NVCC_LVDS	LVDS	ALT0	ldb_LVDS1_TX0	Input	Keeper
LVDS1_TX1_N	AA2	NVCC_LVDS	LVDS		LVDS1_TX1_N	—	—
LVDS1_TX1_P	AA1	NVCC_LVDS	LVDS	ALT0	ldb_LVDS1_TX1	Input	Keeper
LVDS1_TX2_N	AB1	NVCC_LVDS	LVDS		LVDS1_TX2_N	—	—
LVDS1_TX2_P	AB2	NVCC_LVDS	LVDS	ALT0	ldb_LVDS1_TX2	Input	Keeper
LVDS1_TX3_N	AA3	NVCC_LVDS	LVDS		LVDS1_TX3_N	—	—
LVDS1_TX3_P	AA4	NVCC_LVDS	LVDS	ALT0	ldb_LVDS1_TX3	Input	Keeper

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
MLB_CN[2]	A11	MLB	LVDS		MLB_CN	—	—
MLB_CP[2]	B11	MLB	LVDS		MLB_CP	—	—
MLB_DN[2]	B10	MLB	LVDS		MLB_DN	—	—
MLB_DP[2]	A10	MLB	LVDS		MLB_DP	—	—
MLB_SN[2]	A9	MLB	LVDS		MLB_SN	—	—
MLB_SP[2]	B9	MLB	LVDS		MLB_SP	—	—
NANDF_ALE	A16	NVCC_NANDF	GPIO	ALT5	gpio6_GPIO[8]	Input	PU (100K)
NANDF_CLE	C15	NVCC_NANDF	GPIO	ALT5	gpio6_GPIO[7]	Input	PU (100K)
NANDF_CS0	F15	NVCC_NANDF	GPIO	ALT5	gpio6_GPIO[11]	Input	PU (100K)
NANDF_CS1	C16	NVCC_NANDF	GPIO	ALT5	gpio6_GPIO[14]	Input	PU (100K)
NANDF_CS2	A17	NVCC_NANDF	GPIO	ALT5	gpio6_GPIO[15]	Input	PU (100K)
NANDF_CS3	D16	NVCC_NANDF	GPIO	ALT5	gpio6_GPIO[16]	Input	PU (100K)
NANDF_D0	A18	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[0]	Input	PU (100K)
NANDF_D1	C17	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[1]	Input	PU (100K)
NANDF_D2	F16	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[2]	Input	PU (100K)
NANDF_D3	D17	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[3]	Input	PU (100K)
NANDF_D4	A19	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[4]	Input	PU (100K)
NANDF_D5	B18	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[5]	Input	PU (100K)
NANDF_D6	E17	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[6]	Input	PU (100K)
NANDF_D7	C18	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[7]	Input	PU (100K)
NANDF_RB0	B16	NVCC_NANDF	GPIO	ALT5	gpio6_GPIO[10]	Input	PU (100K)
NANDF_WP_B	E15	NVCC_NANDF	GPIO	ALT5	gpio6_GPIO[9]	Input	PU (100K)
ONOFF	D12	VDD_SNVS_IN	GPIO		src_ONOFF	—	—
PCIe_RXM	B1	PCIE			PCIe_RXM	—	—
PCIe_RXP	B2	PCIE			PCIe_RXP	—	—
PCIe_TXM	A3	PCIE			PCIe_TXM	—	—
PCIe_TXP	B3	PCIE			PCIe_TXP	—	—
PMIC_ON_REQ	D11	VDD_SNVS_IN	GPIO	ALT0	snvs_lp_wrapper_SNVS_WAKEUP_ALARM	Output	Open Drain with PU (100K)

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
PMIC_STBY_REQ	F11	VDD_SNVS_IN	GPIO	ALT0	ccm_PMIC_VSTBY_REQ	Output	0
POR_B	C11	VDD_SNVS_IN	GPIO	ALT0	src_POR_B	Input	PU (100K)
RGMII_RD0	C24	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[25]	Input	PU (100K)
RGMII_RD1	B23	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[27]	Input	PU (100K)
RGMII_RD2	B24	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[28]	Input	PU (100K)
RGMII_RD3	D23	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[29]	Input	PU (100K)
RGMII_RX_CTL	D22	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[24]	Input	PD (100K)
RGMII_RXC	B25	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[30]	Input	PD (100K)
RGMII_TD0	C22	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[20]	Input	PU (100K)
RGMII_TD1	F20	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[21]	Input	PU (100K)
RGMII_TD2	E21	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[22]	Input	PU (100K)
RGMII_TD3	A24	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[23]	Input	PU (100K)
RGMII_TX_CTL	C23	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[26]	Input	PD (100K)
RGMII_TXC	D21	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[19]	Input	PD (100K)
RTC_XTALI	D9	ANATOP			RTC_XTALI	—	—
RTC_XTALO	C9	ANATOP			RTC_XTALO	—	—
SATA_RXM	A14	SATA			SATA_RXM	—	—
SATA_RXP	B14	SATA			SATA_RXP	—	—
SATA_TXM	B12	SATA			SATA_TXM	—	—
SATA_TXP	A12	SATA			SATA_TXP	—	—
SD1_CLK	D20	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[20]	Input	PU (100K)
SD1_CMD	B21	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[18]	Input	PU (100K)
SD1_DAT0	A21	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[16]	Input	PU (100K)
SD1_DAT1	C20	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[17]	Input	PU (100K)
SD1_DAT2	E19	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[19]	Input	PU (100K)
SD1_DAT3	F18	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[21]	Input	PU (100K)
SD2_CLK	C21	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[10]	Input	PU (100K)
SD2_CMD	F19	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[11]	Input	PU (100K)
SD2_DAT0	A22	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[15]	Input	PU (100K)
SD2_DAT1	E20	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[14]	Input	PU (100K)

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
SD2_DAT2	A23	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[13]	Input	PU (100K)
SD2_DAT3	B22	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[12]	Input	PU (100K)
SD3_CLK	D14	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[3]	Input	PU (100K)
SD3_CMD	B13	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[2]	Input	PU (100K)
SD3_DAT0	E14	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[4]	Input	PU (100K)
SD3_DAT1	F14	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[5]	Input	PU (100K)
SD3_DAT2	A15	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[6]	Input	PU (100K)
SD3_DAT3	B15	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[7]	Input	PU (100K)
SD3_DAT4	D13	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[1]	Input	PU (100K)
SD3_DAT5	C13	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[0]	Input	PU (100K)
SD3_DAT6	E13	NVCC_SD3	GPIO	ALT5	gpio6_GPIO[18]	Input	PU (100K)
SD3_DAT7	F13	NVCC_SD3	GPIO	ALT5	gpio6_GPIO[17]	Input	PU (100K)
SD3_RST	D15	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[8]	Input	PU (100K)
SD4_CLK	E16	NVCC_NANDF	GPIO	ALT5	gpio7_GPIO[10]	Input	PU (100K)
SD4_CMD	B17	NVCC_NANDF	GPIO	ALT5	gpio7_GPIO[9]	Input	PU (100K)
SD4_DAT0	D18	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[8]	Input	PU (100K)
SD4_DAT1	B19	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[9]	Input	PU (100K)
SD4_DAT2	F17	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[10]	Input	PU (100K)
SD4_DAT3	A20	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[11]	Input	PU (100K)
SD4_DAT4	E18	NVCC_NANDF	GPIO	ALT5	gpio2_PIO[12]	Input	PU (100K)
SD4_DAT5	C19	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[13]	Input	PU (100K)
SD4_DAT6	B20	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[14]	Input	PU (100K)
SD4_DAT7	D19	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[15]	Input	PU (100K)
TAMPER	E11	VDD_SNVS_IN	GPIO	ALT0	snvs_lp_wrapper_SNVS_TD1	Input	PD (100K)
TEST_MODE	E12				Reserved—Factory Use Only	—	—
USB_H1_DN	F10	ANATOP			USB_H1_DN	—	—
USB_H1_DP	E10	ANATOP			USB_H1_DP	—	—
USB_H1_VBUS	D10	ANATOP			USB_H1_VBUS	—	—

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
USB_OTG_CHD_B	B8	ANATOP			USB_OTG_CHD_B	—	—
USB_OTG_DN	B6	ANATOP			USB_OTG_DN	—	—
USB_OTG_DP	A6	ANATOP			USB_OTG_DP	—	—
USB_OTG_VBUS	E9	ANATOP			USB_OTG_VBUS	—	—
XTALI	A7	ANATOP			XTALI	—	—
XTALO	B7	ANATOP			XTALO	—	—
ZQPAD	AE17	NVCC_DRAM	ZQPAD		ZQPAD	Input	Hi-Z

1 The state immediately after reset and before ROM firmware or software has executed.

2 MLB is only supported in automotive graded parts. These balls should be considered as not connected in consumer graded parts.

6.1.3 21 x 21 mm, 0.8 mm Pitch Ball Map

Table 97 shows the FCPBGA 21 x 21 mm, 0.8 mm pitch ball map.

Table 97. 21 x 21 mm, 0.8 mm Pitch Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
A		PCIE_REXT	PCIE_TXM	GND	FA_ANA	USB_OTG_DP	XTALI	GND	MLB_SN	MLB_DP	MLB_CN	SATA_TXP	GND	SATA_RXM	SD3_DAT2	NANDF_ALE	NANDF_CS2	NANDF_D0	NANDF_D4	SD4_DAT3	SD1_DAT0	SD2_DAT0	SD2_DAT2	RGMII_TD3	GND
B	PCIE_RXM	PCIE_RXP	PCIE_TXP	GND	VDD_FA	USB_OTG_DN	XTALO	USB_OTG_CHD_B	MLB_SP	MLB_DN	MLB_CP	SATA_TXM	SD3_CMD	SATA_RXP	SD3_DAT3	NANDF_RB0	SD4_CMD	NANDF_D5	SD4_DAT1	SD4_DAT6	SD1_CMD	SD2_DAT3	RGMII_RD1	RGMII_RD2	RGMII_RXC
C	GND	JTAG_TRSTB	JTAG_TMS	GND	CLK2_N	GND	CLK1_N	GPANAIO	RTC_XTALO	GND	POR_B	BOOT_MODE0	SD3_DAT5	SATA_REXT	NANDF_CLE	NANDF_CS1	NANDF_D1	NANDF_D7	SD4_DAT5	SD1_DAT1	SD2_CLK	RGMII_TD0	RGMII_TX_CTL	RGMII_RD0	EIM_D16

Table 97. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

K	J	H	G	F	E	D
HDMI_HPD	HDMI_REF	DSI_D1P	DSI_D0P	CSI_D3P	CSI_D2M	CSI_D1M
HDMI_DDCCEC	GND	DSI_D1M	DSI_D0M	CSI_D3M	CSI_D2P	CSI_D1P
HDMI_D2M	HDMI_D1M	DSI_CLK0M	GND	CSI_CLK0P	CSI_D0P	GND
HDMI_D2P	HDMI_D1P	DSI_CLK0P	DSI_REXT	CSI_CLK0M	CSI_D0M	CSI_REXT
HDMI_D0M	HDMI_CLKM	JTAG_TCK	JTAG_TDI	GND	GND	CLK2_P
HDMI_D0P	HDMI_CLKP	JTAG_MOD	JTAG_TDO	GND	GND	GND
NVCC_MIPI	NVCC_JTAG	PCIE_VP	PCIE_VPH	GND	GND	CLK1_P
GND	GND	GND	PCIE_VPTX	GND	NVCC_PLL_OUT	GND
VDDARM23_IN	VDDHIGH_IN	VDDHIGH_IN	VDD_SNVS_CAP	VDDUSB_CAP	USB_OTG_VBUS	RTC_XTALI
GND	VDDHIGH_CAP	VDDHIGH_CAP	GND	USB_H1_DN	USB_H1_DP	USB_H1_VBUS
VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP	VDD_SNVS_IN	PMIC_STBY_REQ	TAMPER	PMIC_ON_REQ
GND	GND	GND	SATA_VPH	BOOT_MODE1	TEST_MODE	ONOFF
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	SATA_VP	SD3_DAT7	SD3_DAT6	SD3_DAT4
VDDARM_IN	VDDARM_IN	VDDARM_IN	NVCC_SD3	SD3_DAT1	SD3_DAT0	SD3_CLK
GND	GND	GND	NVCC_NANDF	NANDF_CS0	NANDF_WP_B	SD3_RST
VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	NVCC_SD1	NANDF_D2	SD4_CLK	NANDF_CS3
VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	NVCC_SD2	SD4_DAT2	NANDF_D6	NANDF_D3
GND	GND	GND	NVCC_RGMII	SD1_DAT3	SD4_DAT4	SD4_DAT0
NVCC_EIM0	EIM_D29	EIM_A25	GND	SD2_CMD	SD1_DAT2	SD4_DAT7
EIM_RW	EIM_D30	EIM_D21	EIM_D20	RGMII_TD1	SD2_DAT1	SD1_CLK
EIM_EB0	EIM_A23	EIM_D31	EIM_D19	EIM_D17	RGMII_TD2	RGMII_TXC
EIM_LBA	EIM_A18	EIM_A20	EIM_D25	EIM_D24	EIM_EB2	RGMII_RX_CTL
EIM_EB1	EIM_CS1	EIM_A21	EIM_D28	EIM_EB3	EIM_D22	RGMII_RD3
EIM_DA3	EIM_OE	EIM_CS0	EIM_A17	EIM_A22	EIM_D26	EIM_D18
EIM_DA6	EIM_DA1	EIM_A16	EIM_A19	EIM_A24	EIM_D27	EIM_D23

Table 97. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

V	U	T	R	P	N	M	L
LVDS0_TX2_P	LVDS0_TX0_P	GPIO_2	GPIO_17	CSI0_PIXCLK	CSI0_DAT4	CSI0_DAT10	CSI0_DAT13
LVDS0_TX2_N	LVDS0_TX0_N	GPIO_9	GPIO_16	CSI0_DAT5	CSI0_VSYNC	CSI0_DAT12	GND
LVDS0_CLK_P	LVDS0_TX1_P	GPIO_6	GPIO_7	CSI0_DATA_EN	CSI0_DAT7	CSI0_DAT11	CSI0_DAT17
LVDS0_CLK_N	LVDS0_TX1_N	GPIO_1	GPIO_5	CSI0_MCLK	CSI0_DAT6	CSI0_DAT14	CSI0_DAT16
KEY_ROW4	KEY_COL3	GPIO_0	GPIO_8	GPIO_19	CSI0_DAT9	CSI0_DAT15	GND
KEY_ROW0	KEY_ROW1	KEY_COL4	GPIO_4	GPIO_18	CSI0_DAT8	CSI0_DAT18	CSI0_DAT19
NVCC_LVDS2P5	KEY_COL1	KEY_ROW3	GPIO_3	NVCC_GPIO	NVCC_CSI	HDMI_VPH	HDMI_VP
GND	GND	GND	GND	GND	GND	GND	GND
NVCC_DRAM	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN
NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDSOC_CAP	GND	GND	GND	GND
NVCC_DRAM	GND	GND	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP
NVCC_DRAM	GND	GND	GND	GND	VDD_CACHE_CAP	GND	GND
NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN
NVCC_DRAM	GND	GND	GND	GND	GND	GND	GND
NVCC_DRAM	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN
NVCC_DRAM	GND	GND	GND	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP
NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	GND	GND	GND	GND
GND	GND	GND	NVCC_ENET	NVCC_LCD	DI0_DISP_CLK	NVCC_EIM2	NVCC_EIM1
ENET_MDC	ENET_TXD0	DISP0_DAT21	DISP0_DAT13	DISP0_DAT4	DI0_PIN3	EIM_DA11	EIM_DA0
ENET_TX_EN	ENET_CRS_DV	DISP0_DAT16	DISP0_DAT10	DISP0_DAT3	DI0_PIN15	EIM_DA9	EIM_DA2
ENET_REF_CLK	DISP0_DAT20	DISP0_DAT15	DISP0_DAT8	DISP0_DAT1	EIM_BCLK	EIM_DA10	EIM_DA4
ENET_MDIO	DISP0_DAT19	DISP0_DAT11	DISP0_DAT6	DISP0_DAT2	EIM_DA14	EIM_DA13	EIM_DA5
DISP0_DAT22	DISP0_DAT17	DISP0_DAT12	DISP0_DAT7	DISP0_DAT0	EIM_DA15	EIM_DA12	EIM_DA8
DISP0_DAT18	DISP0_DAT14	DISP0_DAT9	DISP0_DAT5	DI0_PIN4	DI0_PIN2	EIM_WAIT	EIM_DA7

Table 97. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

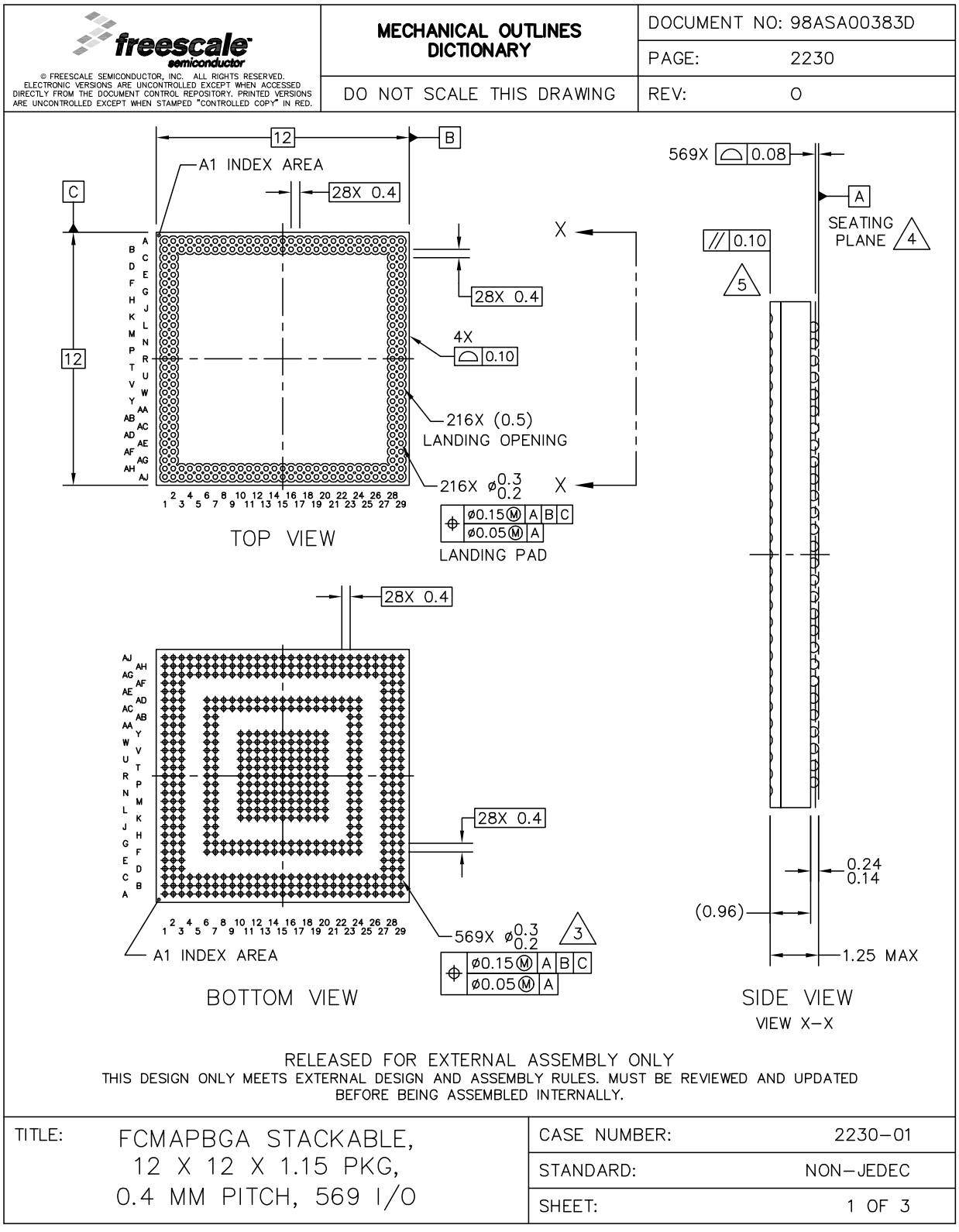
AE	AD	AC	AB	AA	Y	W
GND	DRAM_D5	DRAM_D4	LVDS1_TX2_N	LVDS1_TX1_P	LVDS1_TX0_N	LVDS0_TX3_P
DRAM_D1	DRAM_D0	DRAM_VREF	LVDS1_TX2_P	LVDS1_TX1_N	LVDS1_TX0_P	LVDS0_TX3_N
DRAM_SDQS0	DRAM_SDQS0_B	DRAM_DQM0	GND	LVDS1_TX3_N	LVDS1_CLK_N	GND
DRAM_D7	GND	DRAM_D2	DRAM_D6	LVDS1_TX3_P	LVDS1_CLK_P	KEY_ROW2
DRAM_D9	DRAM_D8	DRAM_D13	DRAM_D12	DRAM_D3	GND	KEY_COL0
DRAM_SDQS1_B	DRAM_SDQS1	DRAM_DQM1	DRAM_D14	DRAM_D10	DRAM_RESET	KEY_COL2
DRAM_D11	GND	DRAM_D15	DRAM_D16	GND	DRAM_D20	GND
DRAM_SDQS2_B	DRAM_SDQS2	DRAM_D22	DRAM_DQM2	DRAM_D17	DRAM_D21	GND
DRAM_D24	DRAM_D29	DRAM_D28	DRAM_D18	DRAM_D23	DRAM_D19	GND
DRAM_DQM3	GND	DRAM_SDQS3	DRAM_SDQS3_B	GND	DRAM_D25	GND
DRAM_D26	DRAM_D30	DRAM_D31	DRAM_D27	DRAM_SDCKE1	DRAM_SDCKE0	GND
DRAM_A9	DRAM_A12	DRAM_A11	DRAM_SDBA2	DRAM_A14	DRAM_A15	GND
DRAM_A5	GND	DRAM_A6	DRAM_A8	GND	DRAM_A7	GND
DRAM_SDCLK_1_B	DRAM_SDCLK_1	DRAM_A0	DRAM_A1	DRAM_A2	DRAM_A3	DRAM_A4
DRAM_SDCLK_0_B	DRAM_SDCLK_0	DRAM_SDBA0	DRAM_RAS	DRAM_A10	DRAM_SDBA1	GND
DRAM_CAS	GND	DRAM_SDODT0	DRAM_SDWE	GND	DRAM_CS0	GND
ZQPAD	DRAM_CS1	DRAM_A13	DRAM_SDODT1	DRAM_D32	DRAM_D36	GND
DRAM_SDQS4_B	DRAM_SDQS4	DRAM_D34	DRAM_DQM4	DRAM_D33	DRAM_D37	GND
DRAM_D35	GND	DRAM_D39	DRAM_D38	GND	DRAM_D40	GND
DRAM_SDQS5_B	DRAM_SDQS5	DRAM_DQM5	DRAM_D41	DRAM_D45	DRAM_D44	ENET_TXD1
DRAM_D46	DRAM_D43	DRAM_D47	DRAM_D42	DRAM_D57	DRAM_DQM7	ENET_RXD0
DRAM_D49	GND	DRAM_D48	DRAM_D52	GND	DRAM_D59	ENET_RXD1
DRAM_SDQS6_B	DRAM_SDQS6	DRAM_D53	DRAM_D60	DRAM_D61	DRAM_D62	ENET_RX_ER
DRAM_D50	DRAM_DQM6	DRAM_D51	GND	DRAM_SDQS7_B	GND	DISP0_DAT23
GND	DRAM_D54	DRAM_D55	DRAM_D56	DRAM_SDQS7	DRAM_D58	DRAM_D63

6.2 12 x 12 mm Package on Package (PoP) Information

This section contains the outline drawing, signal assignment map, ground/power reference ID (by ball grid location) for the 12 x 12 mm, 0.4 mm pitch PoP package.

6.2.1 Case PoP, 0.4 mm Pitch, 12 x 12 Ball Matrix

Figure 109 shows the top, bottom, and side views of the 12 x 12 mm PoP package.



freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASA00383D
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NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK AND LANDING PADS ON TOP SURFACE OF PACKAGE.

TITLE:	FCMAPBGA STACKABLE, 12 X 12 X 1.15 PKG, 0.4 MM PITCH, 569 I/O	CASE NUMBER:	2230–01
		STANDARD:	NON–JEDEC
		SHEET:	2

Figure 109. 12 x 12 mm PoP Package Top, Bottom, and Side Views

6.2.2 12 x 12 mm PoP Ground, Power, Sense, and Reference Contact Assignments

Table 98 and Table 99 show the device connection list for ground, power, sense, and reference contact signals alpha-sorted by name.

Table 98. 12 x 12 mm PoP Top Ground, Power, Sense, and Reference Contact Assignments

Contact Name	Contact Assignment
DRAM_VREF	AH16,B15,R2,U28
DRAM_CA0P0	R29
DRAM_CA0P1	AJ27
DRAM_CA1P0	T29
DRAM_CA1P1	AH27
DRAM_CA2P0	U29
DRAM_CA2P1	AH26
DRAM_CA3P0	V29
DRAM_CA3P1	AH25
DRAM_CA4P0	W28
DRAM_CA4P1	AJ25
DRAM_CA5P0	AC29
DRAM_CA5P1	AJ20
DRAM_CA6P0	AD29
DRAM_CA6P1	AH20
DRAM_CA7P0	AD28
DRAM_CA7P1	AH19
DRAM_CA8P0	AE28
DRAM_CA8P1	AJ18
DRAM_CA9P0	AF29
DRAM_CA9P1	AH17
DRAM_CKE0P0	AA29
DRAM_CKE0P1	AH23
DRAM_CKE1P0	Y29
DRAM_CKE1P1	AJ23
DRAM_CLKP0	AB28
DRAM_CLKP0_B	AB29
DRAM_CLKP1	AJ21
DRAM_CLKP1_B	AH21

Table 98. 12 x 12 mm PoP Top Ground, Power, Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
DRAM_CS0P0	Y28
DRAM_CS0P1	AH24
DRAM_CS1P0	W29
DRAM_CS1P1	AJ24
DRAM_D0P0	U2
DRAM_D0P1	B3
DRAM_D10P0	AG1
DRAM_D10P1	B19
DRAM_D11P0	AH6
DRAM_D11P1	A12
DRAM_D12P0	AE1
DRAM_D12P1	A19
DRAM_D13P0	AG2
DRAM_D13P1	A17
DRAM_D14P0	AF1
DRAM_D14P1	B12
DRAM_D15P0	AJ5
DRAM_D15P1	B17
DRAM_D16P0	H2
DRAM_D16P1	E29
DRAM_D17P0	F2
DRAM_D17P1	A24
DRAM_D18P0	C2
DRAM_D18P1	A27
DRAM_D19P0	E1
DRAM_D19P1	A26
DRAM_D1P0	N1
DRAM_D1P1	A7
DRAM_D20P0	H1
DRAM_D20P1	B27
DRAM_D21P0	G1
DRAM_D21P1	D28
DRAM_D22P0	E2

Table 98. 12 x 12 mm PoP Top Ground, Power, Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
DRAM_D22P1	B26
DRAM_D23P0	D1
DRAM_D23P1	A25
DRAM_D24P0	AH11
DRAM_D24P1	K28
DRAM_D25P0	AJ9
DRAM_D25P1	N29
DRAM_D26P0	AJ14
DRAM_D26P1	H29
DRAM_D27P0	AJ12
DRAM_D27P1	L28
DRAM_D28P0	AH10
DRAM_D28P1	M29
DRAM_D29P0	AJ10
DRAM_D29P1	N28
DRAM_D2P0	M1
DRAM_D2P1	A4
DRAM_D30P0	AJ13
DRAM_D30P1	K29
DRAM_D31P0	AH13
DRAM_D31P1	J29
DRAM_D3P0	Y2
DRAM_D3P1	B5
DRAM_D4P0	V1
DRAM_D4P1	A5
DRAM_D5P0	W1
DRAM_D5P1	A8
DRAM_D6P0	W2
DRAM_D6P1	B8
DRAM_D7P0	L2
DRAM_D7P1	B6
DRAM_D8P0	AJ3
DRAM_D8P1	A18

Table 98. 12 x 12 mm PoP Top Ground, Power, Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
DRAM_D9P0	AH4
DRAM_D9P1	A13
DRAM_DM0P0	AB1
DRAM_DM0P1	B11
DRAM_DM1P0	AC2
DRAM_DM1P1	A21
DRAM_DM2P0	L1
DRAM_DM2P1	B22
DRAM_DM3P0	AH7
DRAM_DM3P1	F28
DRAM_DQS0P0	AA1
DRAM_DQS0P0_B	AA2
DRAM_DQS0P1	B10
DRAM_DQS0P1_B	A10
DRAM_DQS1P0	AD2
DRAM_DQS1P0_B	AD1
DRAM_DQS1P1	A20
DRAM_DQS1P1_B	B20
DRAM_DQS2P0	K2
DRAM_DQS2P0_B	K1
DRAM_DQS2P1	A23
DRAM_DQS2P1_B	B23
DRAM_DQS3P0	AH8
DRAM_DQS3P0_B	AJ8
DRAM_DQS3P1	G28
DRAM_DQS3P1_B	G29
GND	A11,A14,A2,A28,A6,A9,AA28,AB2,AE2,AF28,AH1,AH14,AH18,AH29,AH5,AJ11,AJ16,AJ2,AJ22, AJ28,AJ7,B1,B14,B21,B24,B29,E28,F1,H28,J1,L29,M2,P1,P2,R28,V2,V28
POP_VDD1__1	B2,C1
POP_VDD1__2	A15
POP_VDD1__3	B28,C28
POP_VDD1__4	N2,R1
POP_VDD1__5	P29

Table 98. 12 x 12 mm PoP Top Ground, Power, Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
POP_VDD1__6	AH2
POP_VDD1__7	AJ15
POP_VDD1__8	AH28
POP_VDD2__1	A3
POP_VDD2__2	A16,B16
POP_VDD2__3	C29
POP_VDD2__4	P28
POP_VDD2__5	T1,T2
POP_VDD2__6	AH3
POP_VDD2__7	AH15
POP_VDD2__8	AG28
POP_VDDCA	AC28,AE29,AH22,AJ19,AJ26,T28
POP_VDDQ	A22,AC1,AF2,AH12,AH9,AJ4,AJ6,B13,B18,B25,B4,B7,B9,D2,D29,F29,G2,J2,J28,M28,U1,Y1
POP_ZQP0	AG29
POP_ZQP1	AJ17

Table 99. 12 x 12 mm PoP Bottom Ground, Power, Sense, and Reference Contact Assignments

Contact Name	Contact Assignment
BOOT_MODE0	C14
BOOT_MODE1	G13
CLK1_N	A7
CLK1_P	B7
CLK2_N	A6
CLK2_P	B6
CSI_CLK0M	E2
CSI_CLK0P	E1
CSI_D0M	C2
CSI_D0P	C1
CSI_D1M	D1
CSI_D1P	D2
CSI_D2M	F1
CSI_D2P	F2
CSI_D3M	G2

Table 99. 12 x 12 mm PoP Bottom Ground, Power, Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
CSI_D3P	G1
CSI_REXT	H6
CSI0_DAT10	W3
CSI0_DAT11	V1
CSI0_DAT12	V3
CSI0_DAT13	T6
CSI0_DAT14	U2
CSI0_DAT15	V2
CSI0_DAT16	T2
CSI0_DAT17	U1
CSI0_DAT18	T1
CSI0_DAT19	R3
CSI0_DAT4	U6
CSI0_DAT5	U7
CSI0_DAT6	Y1
CSI0_DAT7	Y2
CSI0_DAT8	W2
CSI0_DAT9	W1
CSI0_DATA_EN	V6
CSI0_MCLK	AA2
CSI0_PIXCLK	AD1
CSI0_VSYNC	AA1
DI0_DISP_CLK	AF29
DI0_PIN15	AD28
DI0_PIN2	AD29
DI0_PIN3	W24
DI0_PIN4	U24
DISP0_DAT0	AH29
DISP0_DAT1	AD27
DISP0_DAT10	AH26
DISP0_DAT11	AJ27
DISP0_DAT12	AF28
DISP0_DAT13	AJ25

Table 99. 12 x 12 mm PoP Bottom Ground, Power, Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
DISP0_DAT14	AJ28
DISP0_DAT15	AH25
DISP0_DAT16	AB24
DISP0_DAT17	AH28
DISP0_DAT18	AH24
DISP0_DAT19	AA24
DISP0_DAT2	AB27
DISP0_DAT20	AD24
DISP0_DAT21	AC24
DISP0_DAT22	Y24
DISP0_DAT23	AJ24
DISP0_DAT3	V23
DISP0_DAT4	V24
DISP0_DAT5	AH27
DISP0_DAT6	U23
DISP0_DAT7	AE28
DISP0_DAT8	AJ26
DISP0_DAT9	AG28
DRAM_CKE0P0	AA29
DRAM_CKE0P1	AH23
DRAM_CKE1P0	Y29
DRAM_CKE1P1	AJ23
DRAM_VREF	AG10
DSI_CLK0M	J1
DSI_CLK0P	J2
DSI_D0M	H2
DSI_D0P	H1
DSI_D1M	K2
DSI_D1P	K1
DSI_REXT	K6
EIM_A16	T29
EIM_A17	N24
EIM_A18	M24

Table 99. 12 x 12 mm PoP Bottom Ground, Power, Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
EIM_A19	R28
EIM_A20	R29
EIM_A21	P29
EIM_A22	P28
EIM_A23	N28
EIM_A24	N27
EIM_A25	H28
EIM_BCLK	AA27
EIM_CS0	U29
EIM_CS1	U28
EIM_D16	J24
EIM_D17	H29
EIM_D18	J28
EIM_D19	J29
EIM_D20	J23
EIM_D21	K29
EIM_D22	K28
EIM_D23	K24
EIM_D24	L29
EIM_D25	L28
EIM_D26	L27
EIM_D27	M28
EIM_D28	M29
EIM_D29	L24
EIM_D30	N29
EIM_D31	L23
EIM_DA0	V28
EIM_DA1	V27
EIM_DA10	Y28
EIM_DA11	AE29
EIM_DA12	Y27
EIM_DA13	R23
EIM_DA14	AC28

Table 99. 12 x 12 mm PoP Bottom Ground, Power, Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
EIM_DA15	AA28
EIM_DA2	W29
EIM_DA3	AB29
EIM_DA4	W27
EIM_DA5	W28
EIM_DA6	T24
EIM_DA7	R24
EIM_DA8	AB28
EIM_DA9	AC29
EIM_EB0	N23
EIM_EB1	P24
EIM_EB2	H27
EIM_EB3	K27
EIM_LBA	V29
EIM_OE	T28
EIM_RW	U27
EIM_WAIT	AG29
ENET_CRS_DV	AG23
ENET_MDC	AJ21
ENET_MDIO	AJ22
ENET_REF_CLK	AH21
ENET_RX_ER	AD22
ENET_RXD0	AH22
ENET_RXD1	AH20
ENET_TX_EN	AG24
ENET_TXD0	AD23
ENET_TXD1	AG21
FA_ANA	J7
GND	A15,A29,AG11,AG13,AG5,AG7,AG8,AH11,AH12,AH13,AH14,AH15,AH16,AH17,AH18,AH19,AJ1 ,AJ11,AJ12,AJ13,AJ14,AJ15,AJ16,AJ17,AJ18,AJ2,AJ20,AJ29,B4,C6,D3,F6,F7,H3,K13,K14,K15, L13,L14,L15,L3,L6,M13,M14,M15,M3,M6,N13,N14,N15,N3,N6,P14,R14,R19,R20,T14,T19,T20,U 10,U11,U12,U13,U14,U15,U16,U17,U18,V10,V11,V12,V13,V14,V15,V16,V17,V18,W13,W14,W1 7,W18,Y13,Y14,Y17,Y18
GPANAIO	C10

Table 99. 12 x 12 mm PoP Bottom Ground, Power, Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
GPIO_0	AE2
GPIO_1	AA6
GPIO_16	AB2
GPIO_17	AC2
GPIO_18	AA3
GPIO_19	AB1
GPIO_2	W6
GPIO_3	AE1
GPIO_4	Y6
GPIO_5	AB3
GPIO_6	AC6
GPIO_7	AC1
GPIO_8	V7
GPIO_9	AD2
HDMI_CLKM	L1
HDMI_CLKP	L2
HDMI_D0M	M1
HDMI_D0P	M2
HDMI_D1M	N1
HDMI_D1P	N2
HDMI_D2M	P1
HDMI_D2P	P2
HDMI_DDCCEC	R2
HDMI_HPD	R1
HDMI_REF	P6
HDMI_VP	M7
HDMI_VPH	N7
JTAG_MOD	F3
JTAG_TCK	B1
JTAG_TDI	L7
JTAG_TDO	B2
JTAG_TMS	A2
JTAG_TRSTB	K3

Table 99. 12 x 12 mm PoP Bottom Ground, Power, Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
KEY_COL0	AB6
KEY_COL1	Y7
KEY_COL2	AD7
KEY_COL3	AD6
KEY_COL4	AF1
KEY_ROW0	AB7
KEY_ROW1	AD3
KEY_ROW2	AF2
KEY_ROW3	AE3
KEY_ROW4	AC7
LVDS0_CLK_N	AH4
LVDS0_CLK_P	AJ4
LVDS0_TX0_N	AG2
LVDS0_TX0_P	AG1
LVDS0_TX1_N	AH2
LVDS0_TX1_P	AH1
LVDS0_TX2_N	AH3
LVDS0_TX2_P	AJ3
LVDS0_TX3_N	AH5
LVDS0_TX3_P	AJ5
LVDS1_CLK_N	AJ8
LVDS1_CLK_P	AH8
LVDS1_TX0_N	AJ6
LVDS1_TX0_P	AH6
LVDS1_TX1_N	AH7
LVDS1_TX1_P	AJ7
LVDS1_TX2_N	AJ9
LVDS1_TX2_P	AH9
LVDS1_TX3_N	AJ10
LVDS1_TX3_P	AH10
NANDF_ALE	A20
NANDF_CLE	G17
NANDF_CS0	A21

Table 99. 12 x 12 mm PoP Bottom Ground, Power, Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
NANDF_CS1	F18
NANDF_CS2	C20
NANDF_CS3	B21
NANDF_D0	F19
NANDF_D1	B22
NANDF_D2	B23
NANDF_D3	A23
NANDF_D4	G19
NANDF_D5	A24
NANDF_D6	C23
NANDF_D7	F20
NANDF_RB0	B20
NANDF_WP_B	C19
NVCC_CSI	T7
NVCC_DRAM	AA23,AB23,AC10,AC11,AC12,AC13,AC14,AC15,AC16,AC17,AC18,AC19,AC20,AC21,AC22,AC23,AC8,AC9,AD10,AD11,AD12,AD13,AD14,AD15,AD16,AD17,AD18,AD19,AD20,AD21,AD8,AD9,Y23
NVCC_EIM0	K23
NVCC_EIM1	M23
NVCC_EIM2	P23
NVCC_ENET	W23
NVCC_GPIO	W7
NVCC_JTAG	G6
NVCC_LCD	T23
NVCC_LVDS2P5	AA7,AG14,AG18,AG20
NVCC_MIPI	K7
NVCC_NANDF	G18
NVCC_PLL_OUT	C8
NVCC_RGMII	G23
NVCC_SD1	G21
NVCC_SD2	G22
NVCC_SD3	G16
ONOFF	A13

Table 99. 12 x 12 mm PoP Bottom Ground, Power, Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
PCIE_REXT	A4
PCIE_RXM	B3
PCIE_RXP	A3
PCIE_TXM	A5
PCIE_TXP	B5
PCIE_VP	H7
PCIE_VPH	G7
PCIE_VPTX	G8
PMIC_ON_REQ	A12
PMIC_STBY_REQ	C12
POP_VDD1__1	C3
POP_VDD1__2	C15
POP_VDD1__3	C27
POP_VDD1__4	P3
POP_VDD1__5	R27
POP_VDD1__6	AG3
POP_VDD1__7	AG16
POP_VDD1__8	AG26
POP_VDD2__1	C4
POP_VDD2__2	C16
POP_VDD2__3	D27
POP_VDD2__4	P27
POP_VDD2__5	T3
POP_VDD2__6	AG4
POP_VDD2__7	AG15
POP_VDD2__8	AG27
POP_VDDCA	AC27,AE27,AG19,AG22,AG25,T27
POP_VDDQ	AC3,AF3,AG12,AG6,AG9,C13,C18,C22,C25,C5,C7,C9,E27,E3,G3,J27,J3,M27,U3,Y3
POP_ZQP0	AF27
POP_ZQP1	AG17
POR_B	F13
RGMII_RD0	G27
RGMII_RD1	F29

Table 99. 12 x 12 mm PoP Bottom Ground, Power, Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
RGMII_RD2	H23
RGMII_RD3	G29
RGMII_RX_CTL	F28
RGMII_RXC	H24
RGMII_TD0	C28
RGMII_TD1	E29
RGMII_TD2	G24
RGMII_TD3	F27
RGMII_TX_CTL	G28
RGMII_TXC	C29
RTC_XTALI	B10
RTC_XTALO	A10
SATA_REXT	F15
SATA_RXM	A16
SATA_RXP	B16
SATA_TXM	A14
SATA_TXP	B14
SATA_VP	G15
SATA_VPH	G14
SD1_CLK	C26
SD1_CMD	D28
SD1_DAT0	A27
SD1_DAT1	B27
SD1_DAT2	F22
SD1_DAT3	A28
SD2_CLK	E28
SD2_CMD	D29
SD2_DAT0	B29
SD2_DAT1	F24
SD2_DAT2	B28
SD2_DAT3	F23
SD3_CLK	C17
SD3_CMD	F16

Table 99. 12 x 12 mm PoP Bottom Ground, Power, Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
SD3_DAT0	A18
SD3_DAT1	B18
SD3_DAT2	A19
SD3_DAT3	F17
SD3_DAT4	F14
SD3_DAT5	B17
SD3_DAT6	B15
SD3_DAT7	A17
SD3_RST	B19
SD4_CLK	A22
SD4_CMD	C21
SD4_DAT0	B24
SD4_DAT1	A25
SD4_DAT2	G20
SD4_DAT3	A26
SD4_DAT4	F21
SD4_DAT5	C24
SD4_DAT6	B26
SD4_DAT7	B25
TAMPER	B12
TEST_MODE	B13
USB_H1_DN	B11
USB_H1_DP	A11
USB_H1_VBUS	C11
USB_OTG_CHD_B	F12
USB_OTG_DN	B9
USB_OTG_DP	A9
USB_OTG_VBUS	G11
VDD_CACHE_CAP	P7
VDD_FA	J6
VDD_SNVS_CAP	G9
VDD_SNVS_IN	G12
VDDARM_CAP	P15,P16,P17,P18,R15,R16,R17,R18,T15,T16,T17,T18

Table 99. 12 x 12 mm PoP Bottom Ground, Power, Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
VDDARM_IN	K16,K17,K18,L16,L17,L18,M16,M17,M18,N16,N17,N18
VDDARM23_CAP	P10,P11,P12,P13,R10,R11,R12,R13,T10,T11,T12,T13
VDDARM23_IN	K10,K11,K12,L10,L11,L12,M10,M11,M12,N10,N11,N12
VDDHIGH_CAP	F10.F11
VDDHIGH_IN	F8,F9
VDDPU_CAP	N19,N20,P19,P20,U19,U20,V19,V20
VDDSOC_CAP	K19,K20,R6,R7,W10,W11,W12,W15,W16,Y10,Y11,Y12,Y15,Y16
VDDSOC_IN	L19,L20,M19,M20,W19,W20,Y19,Y20
VDDUSB_CAP	G10
XTALI	A8
XTALO	B8
ZQPAD	AJ19

6.2.3 12 x 12 mm PoP, 0.4 mm Pitch Ball Maps

Table 100 shows the 12 x 12 mm, 0.4 mm pitch top ball map. Table 101 shows the 12 x 12 mm, 0.4 mm pitch bottom ball map.

Table 100. PoP 12 x 12 mm, 0.4 mm Pitch Top Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	DNU	GND	POP_VDD2__1	DRAM_D2P1	DRAM_D4P1	GND	DRAM_D1P1	DRAM_D5P1	GND	DRAM_DQS0P1_B	GND	DRAM_D11P1	DRAM_D9P1	GND	POP_VDD1__2	POP_VDD2__2	DRAM_D13P1	DRAM_D8P1	DRAM_D12P1	DRAM_DQS1P1	DRAM_DM1P1	POP_VDDQ	DRAM_DQS2P1	DRAM_D17P1	DRAM_D23P1	DRAM_D19P1	DRAM_D18P1	GND	DNU
B	GND	POP_VDD1__1	DRAM_D0P1	POP_VDDQ	DRAM_D3P1	DRAM_D7P1	POP_VDDQ	DRAM_D6P1	POP_VDDQ	DRAM_DQS0P1	DRAM_DM0P1	DRAM_D14P1	POP_VDDQ	GND	DRAM_VREF	POP_VDD2__2	DRAM_D15P1	POP_VDDQ	DRAM_D10P1	DRAM_DQS1P1_B	GND	DRAM_DM2P1	DRAM_DQS2P1_B	GND	POP_VDDQ	DRAM_D22P1	DRAM_D20P1	POP_VDD1__3	GND
C	POP_VDD1__1	DRAM_D18P0																										POP_VDD1__3	POP_VDD2__3

Table 100. PoP 12 x 12 mm, 0.4 mm Pitch Top Ball Map (continued)

L	K	J	H	G	F	E	D
DRAM_DM2P0	DRAM_DQS2P0_B	GND	DRAM_D20P0	DRAM_D21P0	GND	DRAM_D19P0	DRAM_D23P0
DRAM_D7P0	DRAM_DQS2P0	POP_VDDQ	DRAM_D16P0	POP_VDDQ	DRAM_D17P0	DRAM_D22P0	POP_VDDQ
DRAM_D27P1	DRAM_D24P1	POP_VDDQ	GND	DRAM_DQS3P1	DRAM_DM3P1	GND	DRAM_D21P1
GND	DRAM_D30P1	DRAM_D31P1	DRAM_D26P1	DRAM_DQS3P1_B	POP_VDDQ	DRAM_D16P1	POP_VDDQ

Table 100. PoP 12 x 12 mm, 0.4 mm Pitch Top Ball Map (continued)

Y	W	V	U	T	R	P	N	M
POP_VDDQ	DRAM_D5P0	DRAM_D4P0	POP_VDDQ	POP_VDD2__5	POP_VDD1__4	GND	DRAM_D1P0	DRAM_D2P0
DRAM_D3P0	DRAM_D6P0	GND	DRAM_D0P0	POP_VDD2__5	DRAM_VREF	GND	POP_VDD1__4	GND
DRAM_CS0P0	DRAM_CA4P0	GND	DRAM_VREF	POP_VDDCA	GND	POP_VDD2__4	DRAM_D29P1	POP_VDDQ
DRAM_CKE1P0	DRAM_CS1P0	DRAM_CA3P0	DRAM_CA2P0	DRAM_CA1P0	DRAM_CA0P0	POP_VDD1__5	DRAM_D25P1	DRAM_D28P1

Table 100. PoP 12 x 12 mm, 0.4 mm Pitch Top Ball Map (continued)

AA	AB	AC	AD	AE	AF	AG
DRAM_DQS0P0	DRAM_DM0P0	POP_VDDQ	DRAM_DQS1P0_B	DRAM_D12P0	DRAM_D14P0	DRAM_D10P0
DRAM_DQS0P0_B	GND	DRAM_DM1P0	DRAM_DQS1P0	GND	POP_VDDQ	DRAM_D13P0
GND	DRAM_CLKP0	POP_VDDCA	DRAM_CA7P0	DRAM_CA8P0	GND	POP_VDD2__8
DRAM_CKE0P0	DRAM_CLKP0_B	DRAM_CA5P0	DRAM_CA6P0	POP_VDDCA	DRAM_CA9P0	POP_ZQP0

Table 100. PoP 12 x 12 mm, 0.4 mm Pitch Top Ball Map (continued)

AJ	AH
DNU	GND
GND	POP_VDD1__6
DRAM_D8P0	POP_VDD2__6
POP_VDDQ	DRAM_D9P0
DRAM_D15P0	GND
POP_VDDQ	DRAM_D11P0
GND	DRAM_DM3P0
DRAM_DQS3P0_B	DRAM_DQS3P0
DRAM_D25P0	POP_VDDQ
DRAM_D29P0	DRAM_D28P0
GND	DRAM_D24P0
DRAM_D27P0	POP_VDDQ
DRAM_D30P0	DRAM_D31P0
DRAM_D26P0	GND
POP_VDD1__7	POP_VDD2__7
GND	DRAM_VREF
POP_ZQP1	DRAM_CA9P1
DRAM_CA8P1	GND
POP_VDDCA	DRAM_CA7P1
DRAM_CA5P1	DRAM_CA6P1
DRAM_CLKP1	DRAM_CLKP1_B
GND	POP_VDDCA
DRAM_CKE1P1	DRAM_CKE0P1
DRAM_CS1P1	DRAM_CS0P1
DRAM_CA4P1	DRAM_CA3P1
POP_VDDCA	DRAM_CA2P1
DRAM_CA0P1	DRAM_CA1P1
GND	POP_VDD1__8
DNU	GND

Table 101. PoP 12 x 12 mm, 0.4 mm Pitch Bottom Ball Map

	A	B	C	D	E
1	NC	JTAG_TCK	CSI_D0P	CSI_D1M	CSI_CLK0P
2	JTAG_TMS	JTAG_TDO	CSI_D0M	CSI_D1P	CSI_CLK0M
3	PCIE_RXP	PCIE_RXM	POP_VDD1__1	GND	POP_VDDQ
4	PCIE_REXT	GND	POP_VDD2__1		
5	PCIE_TXM	PCIE_TXP	POP_VDDQ		
6	CLK2_N	CLK2_P	GND		
7	CLK1_N	CLK1_P	POP_VDDQ		
8	XTALI	XTALO	NVCC_PLL_OUT		
9	USB_OTG_DP	USB_OTG_DN	POP_VDDQ		
10	RTC_XTALO	RTC_XTALI	GPANAIO		
11	USB_H1_DP	USB_H1_DN	USB_H1_VBUS		
12	PMIC_ON_REQ	TAMPER	PMIC_STBY_REQ		
13	ONOFF	TEST_MODE	POP_VDDQ		
14	SATA_TXM	SATA_TXP	BOOT_MODE0		
15	GND	SD3_DAT6	POP_VDD1__2		
16	SATA_RXM	SATA_RXP	POP_VDD2__2		
17	SD3_DAT7	SD3_DAT5	SD3_CLK		
18	SD3_DAT0	SD3_DAT1	POP_VDDQ		
19	SD3_DAT2	SD3_RST	NANDF_WP_B		
20	NANDF_ALE	NANDF_RB0	NANDF_CS2		
21	NANDF_CS0	NANDF_CS3	SD4_CMD		
22	SD4_CLK	NANDF_D1	POP_VDDQ		
23	NANDF_D3	NANDF_D2	NANDF_D6		
24	NANDF_D5	SD4_DAT0	SD4_DAT5		
25	SD4_DAT1	SD4_DAT7	POP_VDDQ		
26	SD4_DAT3	SD4_DAT6	SD1_CLK		
27	SD1_DAT0	SD1_DAT1	POP_VDD1__3	POP_VDD2__3	POP_VDDQ
28	SD1_DAT3	SD2_DAT2	RGMII_TD0	SD1_CMD	SD2_CLK
29	GND	SD2_DAT0	RGMII_TXC	SD2_CMD	RGMII_TD1

Table 101. PoP 12 x 12 mm, 0.4 mm Pitch Bottom Ball Map (continued)

N	M	L	K	J	H	G	F
HDMI_D1M	HDMI_D0M	HDMI_CLKM	DSI_D1P	DSI_CLK0M	DSI_D0P	CSI_D3P	CSI_D2M
HDMI_D1P	HDMI_D0P	HDMI_CLKP	DSI_D1M	DSI_CLK0P	DSI_D0M	CSI_D3M	CSI_D2P
GND	GND	GND	JTAG_TRSTB	POP_VDDQ	GND	POP_VDDQ	JTAG_MOD
GND	GND	GND	DSI_REXT	VDD_FA	CSI_REXT	NVCC_JTAG	GND
HDMI_VPH	HDMI_VP	JTAG_TDI	NVCC_MIPI	FA_ANA	PCIE_VP	PCIE_VPH	GND
						PCIE_VPTX	VDDHIGH_IN
						VDD_SNVS_CAP	VDDHIGH_IN
VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN			VDDUSB_CAP	VDDHIGH_CAP
VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN			USB_OTG_VBUS	VDDHIGH_CAP
VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN			VDD_SNVS_IN	USB_OTG_CHD_B
GND	GND	GND	GND			BOOT_MODE1	POR_B
GND	GND	GND	GND			SATA_VPH	SD3_DAT4
GND	GND	GND	GND			SATA_VP	SATA_REXT
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN			NVCC_SD3	SD3_CMD
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN			NANDF_CLE	SD3_DAT3
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN			NVCC_NANDF	NANDF_CS1
VDDPU_CAP	VDDSOC_IN	VDDSOC_IN	VDDSOC_CAP			NANDF_D4	NANDF_D0
VDDPU_CAP	VDDSOC_IN	VDDSOC_IN	VDDSOC_CAP			SD4_DAT2	NANDF_D7
						NVCC_SD1	SD4_DAT4
						NVCC_SD2	SD1_DAT2
EIM_EB0	NVCC_EIM1	EIM_D31	NVCC_EIM0	EIM_D20	RGMII_RD2	NVCC_RGMII	SD2_DAT3
EIM_A17	EIM_A18	EIM_D29	EIM_D23	EIM_D16	RGMII_RXC	RGMII_TD2	SD2_DAT1
EIM_A24	POP_VDDQ	EIM_D26	EIM_EB3	POP_VDDQ	EIM_EB2	RGMII_RD0	RGMII_TD3
EIM_A23	EIM_D27	EIM_D25	EIM_D22	EIM_D18	EIM_A25	RGMII_TX_CTL	RGMII_RX_CTL
EIM_D30	EIM_D28	EIM_D24	EIM_D21	EIM_D19	EIM_D17	RGMII_RD3	RGMII_RD1

Table 101. PoP 12 x 12 mm, 0.4 mm Pitch Bottom Ball Map (continued)

AA	Y	W	V	U	T	R	P
CSI0_VSYNC	CSI0_DAT6	CSI0_DAT9	CSI0_DAT11	CSI0_DAT17	CSI0_DAT18	HDMI_HPD	HDMI_D2M
CSI0_MCLK	CSI0_DAT7	CSI0_DAT8	CSI0_DAT15	CSI0_DAT14	CSI0_DAT16	HDMI_DDCCEC	HDMI_D2P
GPIO_18	POP_VDDQ	CSI0_DAT10	CSI0_DAT12	POP_VDDQ	POP_VDD2__5	CSI0_DAT19	POP_VDD1__4
GPIO_1	GPIO_4	GPIO_2	CSI0_DATA_EN	CSI0_DAT4	CSI0_DAT13	VDDSOC_CAP	HDMI_REF
NVCC_LVDS2P5	KEY_COL1	NVCC_GPIO	GPIO_8	CSI0_DAT5	NVCC_CSI	VDDSOC_CAP	VDD_CACHE_CAP
	VDDSOC_CAP	VDDSOC_CAP	GND	GND	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP
	VDDSOC_CAP	VDDSOC_CAP	GND	GND	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP
	VDDSOC_CAP	VDDSOC_CAP	GND	GND	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP
	GND	GND	GND	GND	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP
	GND	GND	GND	GND	GND	GND	GND
	VDDSOC_CAP	VDDSOC_CAP	GND	GND	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
	VDDSOC_CAP	VDDSOC_CAP	GND	GND	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
	GND	GND	GND	GND	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
	GND	GND	GND	GND	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
	VDDSOC_IN	VDDSOC_IN	VDDPU_CAP	VDDPU_CAP	GND	GND	VDDPU_CAP
	VDDSOC_IN	VDDSOC_IN	VDDPU_CAP	VDDPU_CAP	GND	GND	VDDPU_CAP
NVCC_DRAM	NVCC_DRAM	NVCC_ENET	DISP0_DAT3	DISP0_DAT6	NVCC_LCD	EIM_DA13	NVCC_EIM2
DISP0_DAT19	DISP0_DAT22	DI0_PIN3	DISP0_DAT4	DI0_PIN4	EIM_DA6	EIM_DA7	EIM_EB1
EIM_BCLK	EIM_DA12	EIM_DA4	EIM_DA1	EIM_RW	POP_VDDCA	POP_VDD1__5	POP_VDD2__4
EIM_DA15	EIM_DA10	EIM_DA5	EIM_DA0	EIM_CS1	EIM_OE	EIM_A19	EIM_A22
DRAM_CKE0P0	DRAM_CKE1P0	EIM_DA2	EIM_LBA	EIM_CS0	EIM_A16	EIM_A20	EIM_A21

Table 101. PoP 12 x 12 mm, 0.4 mm Pitch Bottom Ball Map (continued)

AJ	AH	AG	AF	AE	AD	AC	AB
GND	LVDS0_TX1_P	LVDS0_TX0_P	KEY_COL4	GPIO_3	CSI0_PIXCLK	GPIO_7	GPIO_19
GND	LVDS0_TX1_N	LVDS0_TX0_N	KEY_ROW2	GPIO_0	GPIO_9	GPIO_17	GPIO_16
LVDS0_TX2_P	LVDS0_TX2_N	POP_VDD1__6	POP_VDDQ	KEY_ROW3	KEY_ROW1	POP_VDDQ	GPIO_5
LVDS0_CLK_P	LVDS0_CLK_N	POP_VDD2__6					
LVDS0_TX3_P	LVDS0_TX3_N	GND					
LVDS1_TX0_N	LVDS1_TX0_P	POP_VDDQ			KEY_COL3	GPIO_6	KEY_COL0
LVDS1_TX1_P	LVDS1_TX1_N	GND			KEY_COL2	KEY_ROW4	KEY_ROW0
LVDS1_CLK_N	LVDS1_CLK_P	GND			NVCC_DRAM	NVCC_DRAM	
LVDS1_TX2_N	LVDS1_TX2_P	POP_VDDQ			NVCC_DRAM	NVCC_DRAM	
LVDS1_TX3_N	LVDS1_TX3_P	DRAM_VREF			NVCC_DRAM	NVCC_DRAM	
GND	GND	GND			NVCC_DRAM	NVCC_DRAM	
GND	GND	POP_VDDQ			NVCC_DRAM	NVCC_DRAM	
GND	GND	GND			NVCC_DRAM	NVCC_DRAM	
GND	GND	NVCC_LVDS2P5			NVCC_DRAM	NVCC_DRAM	
GND	GND	POP_VDD2__7			NVCC_DRAM	NVCC_DRAM	
GND	GND	POP_VDD1__7			NVCC_DRAM	NVCC_DRAM	
GND	GND	POP_ZQP1			NVCC_DRAM	NVCC_DRAM	
GND	GND	NVCC_LVDS2P5			NVCC_DRAM	NVCC_DRAM	
ZQPAD	GND	POP_VDDCA			NVCC_DRAM	NVCC_DRAM	
GND	ENET_RXD1	NVCC_LVDS2P5			NVCC_DRAM	NVCC_DRAM	
ENET_MDC	ENET_REF_CLK	ENET_TXD1			NVCC_DRAM	NVCC_DRAM	
ENET_MDIO	ENET_RXD0	POP_VDDCA			ENET_RX_ER	NVCC_DRAM	
DRAM_CKE1P1	DRAM_CKE0P1	ENET_CRS_DV			ENET_TXD0	NVCC_DRAM	NVCC_DRAM
DISP0_DAT23	DISP0_DAT18	ENET_TX_EN			DISP0_DAT20	DISP0_DAT21	DISP0_DAT16
DISP0_DAT13	DISP0_DAT15	POP_VDDCA					
DISP0_DAT8	DISP0_DAT10	POP_VDD1__8					
DISP0_DAT11	DISP0_DAT5	POP_VDD2__8	POP_ZQP0	POP_VDDCA	DISP0_DAT1	POP_VDDCA	DISP0_DAT2
DISP0_DAT14	DISP0_DAT17	DISP0_DAT9	DISP0_DAT12	DISP0_DAT7	DI0_PIN15	EIM_DA14	EIM_DA8
GND	DISP0_DAT0	EIM_WAIT	DI0_DISP_CLK	EIM_DA11	DI0_PIN2	EIM_DA9	EIM_DA3

7 Revision History

Table 102 provides a revision history for this data sheet.

Table 102. i.MX 6Dual/6Quad Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev B	12/2011	• In Table 1, "Ordering Information," on page 3, updated feature information and added part numbers PCIMX6D5EVT10AA, PCIMX6D5EYM10AA, PCIMX6Q5EZK10AA, and PCIMX6D5EZK10AA. • In Section 1.2, “Features,” updated second bullet item under “Camera sensors.” • Removed DTCP references from throughout the document. • In Table 2, "i.MX 6Dual/6Quad Modules List," on page 8, updated Temperature Monitor row. • Added Section 3.1, “Special Signal Considerations.” • Added Section 3.2, “Recommended Connections for Unused Analogue Interfaces.” • In Table 7, "Absolute Maximum Ratings," on page 22, removed VCC absolute maximum ratings and added VDDARM/VDDARM23/VDDSOC and VDDHIGH_IN absolute maximum ratings. • In Table 8, "FCPBGA Package Thermal Resistance Data," on page 22, updated lidded package Junction to Ambient (at 200 ft/min) rating for four layer board. • Added Section 4.1.2.2, “PoP Package Thermal Resistance.” • In Table 10, "Operating Ranges," on page 24. • Added Table 11, "On-Chip Supplies that can be Sourced from LDO Regulators," on page 26. • In Section 4.1.4, “External Clock Sources,” added two new paragraphs at the end of the section. • In Section 4.1.5, “Maximal Supply Currents,” updated the first paragraph. • Updated Table 13, "Maximal Supply Currents," on page 27. • Updated Table 14, "Stop Mode Current and Power Consumption," on page 29. • In Section 4.1.7, “USB PHY Current Consumption,” removed the Normal Mode section and updated Section 4.1.7.1, “Power Down Mode.” • In Table 17, "PCIe2 PHY Power Consumption," on page 31, updated column headings and Mode column entries. • Added Section 4.1.10, “HDMI Typical Power Consumption.” • Updated Section 4.2.1, “Power-Up Sequence.” • In Section 4.3.2.1, “LDO_1P1,” Section 4.3.2.2, “LDO_2P5,” and Section 4.3.2.3, “LDO_USB,” updated the third sentence of the first paragraph. • In Section 4.4, “PLL’s Electrical Characteristics,” updated/added lock time parameter in Table 19, Table 20, Table 21, Table 22, and Table 23. • In Section 4.5.1, “OSC24M,” updated the first paragraph. • In Section 4.5.2, “OSC32K,” updated first and third paragraphs and added a note before Table 24. • In Table 24, "OSC32K Main Characteristics," on page 37, updated the Current consumption row. • In Table 25, "GPIO I/O DC Parameters," on page 38, updated eight TBD values. • In Table 26, "LPDDR2 I/O DC Electrical Parameters," on page 39, added typical and maximum values for the “Input current (no pull-up/down)” parameter. • In Table 27, "DDR3 I/O DC Electrical Parameters," on page 40, added typical and maximum values for the “Input current (no pull-up/down)” parameter. • In Section 4.9, “System Modules Timing,” updated the caution text after the first paragraph. • Updated Table 38, "Reset Timing Parameters," on page 48. • Updated Table 39, "WATCHDOG_RST Timing Parameters," on page 48. • In Table 43, "EIM Asynchronous Timing Parameters Table Relative Chip Select," on page 59, updated TBD value for MAXDTI. • Added Table 68, "Synchronous Display Interface Timing Characteristics (Pixel Level)," on page 109. • Added Section 4.11.21, “USB HSIC Timings.” • Updated Figure 107, "21 x 21 mm Lidded Package Top, Bottom, and Side Views," on page 154. • In Table 95, "21 x 21 mm Supplies Contact Assignment," on page 157, changed supply rail name for ball position A5 from RESERVED to FA_ANA and sorted and formatted the table. • Updated Table 96, "21 x 21 mm Functional Contact Assignments," on page 159. • Added Section 6.1.3, “21 x 21 mm, 0.8 mm Pitch Ball Map.” • Added Section 6.2, “12 x 12 mm Package on Package (PoP) Information.”

Table 102. i.MX 6Dual/6Quad Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev A	07/2011	Initial NDA release.

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