

December 2010

# NC7SZ66 Low Voltage Single SPST Normally Open Bus Switch

## **Features**

- Broad V<sub>CC</sub> Operating Range: 1.65V to 5.5V
- Rail-to-Rail Signal Handling
- Power Down High-Impedance Inputs/Outputs
- 5Ω Switch Connection between Two Ports
- Minimal Propagation Delay through the Switch
- Low Icc
- Zero Bounce in Flow-Through Mode
- Control Input Compatible with CMOS Input Levels
- Ultra-Small MicroPak™ Packages
- Space-Saving SOT23 and SC70 Packages

## Description

The NC7SZ66 is a ultra high-speed (UHS) CMOS compatible single-pole/single-throw (SPST) bus switch. The LOW on resistance of the switch allows inputs to be connected to out-puts with minimal propagation delay and without generating additional ground bounce noise. The device is organized as a 1- bit switch with a switch enable (OE) signal. When OE is HIGH, the switch is on and port A is connected to port B. When OE is LOW, the switch is open and a high-impedance state exists between the two ports..

# **Ordering Information**

Part Number	Top Mark	Package	Packing Method
NC7SZ66M5X	7Z66	5-Lead SOT23, JEDEC MO-178 1.6mm	3000 Units on Tape & Reel
NC7SZ66P5X	Z66	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3000 Units on Tape & Reel
NC7SZ66L6X	EE	6-Lead, MicroPak™, 1x1mm Wide	5000 Units on Tape & Reel

# **Connection Diagrams**

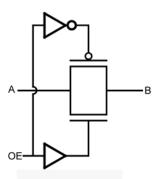
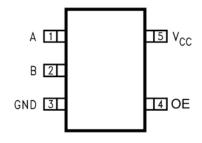
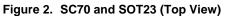


Figure 1. Logic Symbol

# **Pin Configurations**





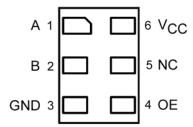


Figure 3. MicroPak™ (Top Through View)

# **Pin Definitions**

Pin # SC70 / SOT23	Pin # MicroPak™	Name	Description
1	1	A	Bus A I/O
2	2	В	Bus B I/O
3	3	GND	Ground
4	4	OE	Switch Enable Input
5	6	Vcc	Supply Voltage
	5	NC	No Connect

# **Function Table**

OE	B <sub>0</sub>	Function
L	High Z-State	Disconnected
Н	A <sub>0</sub>	Connect

H = HIGH Logic Level

L = LOW Logic Level

# **Absolute Maximum Ratings**

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Paran	Parameter		Max.	Unit
V <sub>CC</sub>	Supply Voltage		-0.5	7.0	V
Vs	DC Switch Voltage <sup>(1)</sup>		-0.5	V <sub>CC</sub> to 0.5	V
V <sub>IN</sub>	DC Input Voltage		-0.5	7.0	V
I <sub>IK</sub>	DC Input Diode Current	V <sub>IN</sub> < 0V		-50	mA
lout	DC Output Sink Current			128	mA
I <sub>CC</sub> or I <sub>GND</sub>	DC V <sub>CC</sub> or Ground Current			±100	mA
T <sub>STG</sub>	Storage Temperature Range		-65	+150	°C
TJ	Junction Temperature Under Bia	S		+150	°C
TL	Junction Lead Temperature (Solo	dering, 10 Seconds)		+260	°C
В	Dower Dissipation at 195°C	SOT-23		200	mW
P <sub>D</sub>	Power Dissipation at +85°C	SC70-5		150	IIIVV
ESD	Human Body Model, JEDEC:JES	D22-A114		4000	V
ESD	Charge Device Model: JEDEC:JE	SD22-C101		1500	V

#### Note

# **Recommended Operating Conditions**

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V <sub>CC</sub>	Supply Voltage Operating		1.65	5.50	V
$V_{IN}$	Input Voltage		0	5.5	V
Vs	Switch Input Voltage		0	V <sub>CC</sub>	V
V <sub>OUT</sub>	Output Voltage		0	V <sub>CC</sub>	V
		V <sub>CC</sub> =2.3V - 3.6V	0	10	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Times	V <sub>CC</sub> =4.5V - 5.5V	0	5	ns/V
		Switching I/O	0	DC	
T <sub>A</sub>	Operating Temperature		-40	+85	°C
0	Thermal Resistance	SOT-23		300	°C/W
θЈА	memai Resistance	SC70-5		425	C/VV

#### Note:

2. Unused inputs must be held HIGH or LOW; they may not float.

The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

## **DC Electrical Characteristics**

All typical values are at the specified  $V_{CC}$ , and  $T_A = 25$ °C.

Counch of	Domonoton	V	Conditions	T <sub>A</sub> =-	40 to +8	35°C	T <sub>A</sub> =+	25°C	l leite	
Symbol	Parameter	V <sub>cc</sub>	Conditions		Тур.	Max.	Min.	Тур.	Units	
V	HIGH Level	1.65 to 1.95		0.75V <sub>CC</sub>					V	
V <sub>IH</sub>	Input Voltage	2.30 to 5.50		0.7V <sub>CC</sub>					V	
VIL	LOW Level	1.65 to 1.95				0.25V <sub>CC</sub>			V	
VIL	Input Voltage	2.30 to 5.50				0.3V <sub>CC</sub>			V	
I <sub>IN</sub>	Control Input Leakage Current	0 to 5.5	$0 \le V_{IN} \le 5.5V$		±0.05	±1.00			μA	
I <sub>OFF</sub>	Off Leakage Current	1.65 to 5.50	$0 \le A, B \le V_{CC}$		±0.05	±10.00			μA	
			V <sub>IN</sub> =0V, I <sub>IN</sub> =30mA		3	7				
		4.5	V <sub>IN</sub> =2.4V, I <sub>IN</sub> =15mA		5	12				
	/			V <sub>IN</sub> =4.5V, I <sub>IN</sub> =30mA		7	15			
	0 " 1 0	3.0	V <sub>IN</sub> =0V, I <sub>IN</sub> =24mA		4	9				
Ron	Switch On Resistance <sup>(3)</sup>	3.0	V <sub>IN</sub> =3V, I <sub>IN</sub> =24mA		10	20			Ω	
		2.30	V <sub>IN</sub> =0V, I <sub>IN</sub> =8mA		5	12				
		2.50	V <sub>IN</sub> =2.3V, I <sub>IN</sub> =8mA		13	30				
		1.8	V <sub>IN</sub> =0V, I <sub>IN</sub> =4mA		7	28				
		1.0	V <sub>IN</sub> =1.8V, I <sub>IN</sub> =4mA		25	60				
		5.0	$I_{A}\text{=-}30\text{mA},\\ 0 \leq V_{Bn} \leq V_{CC}$					6		
	On	3.3	$ \begin{aligned} &I_A \!\!=\!\! -24mA, \\ &0 \leq V_{Bn} \leq V_{CC} \end{aligned} $					12		
R <sub>flat</sub>	Resistance Flatness <sup>(3,4,5)</sup>	2.5	$I_A = -8mA, \\ 0 \le V_{Bn} \le V_{CC}$					128	Ω	
		1.8	$I_{A}\text{=-}4mA, \\ 0 \leq V_{Bn} \leq V_{CC}$					125		
Icc	Quiescent Supply Current	1.65 to 5.50	$V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$		0.05	10.00			μA	

#### Notes:

- 3. Measured by the voltage drop between pins A and B at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.
- 4. Parameter is characterized but not tested in production.
- 5. Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.

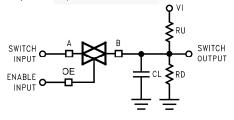
## **AC Electrical Characteristics**

All typical values are at the specified  $V_{CC}$ , and  $T_A = 25$ °C.

Symbol	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		Units	Figure				
				Min.	Тур.	Max.		
		1.65 to 1.95				4.3		
	Propagation Delay	2.3 to 2.7	V <sub>IN</sub> =0PEN			1.2	20	Figure 5
t <sub>PHL</sub> , t <sub>PLH</sub>	Bus-to-Bus <sup>(6)</sup>	3.0 to 3.6	VIN=UPEIN			0.8	ns	Figure 6
		4.5 to 5.5				0.3		
		1.65 to 1.95		1.5	7.0	14.2		
	Output Enable Time	2.5 10 2.1	V <sub>IN</sub> =2 x V <sub>CC</sub> for	1.5	3.3	7.0	ne	Figure 5
$t_{PZL}, t_{PZH}$	Output Enable Time	3.0 to 3.6	$t_{PZL}$ , $V_{IN}$ =0V for $t_{PZH}$	1.5	2.4	5.5	ns	Figure 6
		4.5 to 5.5		1.5	2.0	4.5		
		1.65 to 1.95		1.5	9.2	18.2		
t t	Output Disable Time	2.3 to 2.7	$V_{IN}=2 \times V_{CC}$ for	1.5	5.3	9.0	ns	Figure 5
$t_{PLZ}, t_{PHZ}$	Output Disable Time	3.0 to 3.6	$t_{PLZ}$ , $V_{IN} = 0V$ for $t_{PHZ}$	1.5	4.0	7.0	115	Figure 6
		4.5 to 5.5		1.5	2.7	5.0		
C <sub>IN</sub>	Control Pin Input Capacitance		V <sub>CC</sub> =0		2		pF	
C <sub>I/O</sub>	Input / Output Capacitance		V <sub>CC</sub> =05.0V		6		pF	

#### Note:

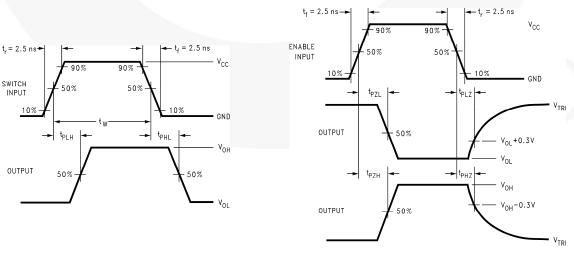
This parameter is guaranteed by design but is not tested. The switch contributes no propagation delay other than the RC delay of the typical on resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).



## Notes:

- 7. Input driven by  $50\Omega$ ; source terminated in  $50\Omega$ .
- 8. C<sub>L</sub> includes load and stray capacitance.
- 9. Input PRR=1.0MHz; t<sub>w</sub>=500ns.

Figure 4. AC Test Circuit



# **Physical Dimensions**

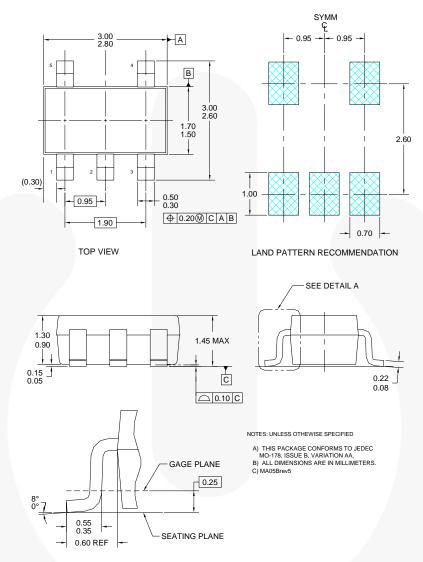


Figure 6. 5-Lead SOT23, JEDEC MO-178 1.6mm

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## **Tape and Reel Specifications**

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: http://www.fairchildsemi.com/packaging/SOT23-5L\_tr.pdf.

Package Designator	Tape Section	<b>Cavity Number</b>	Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
M5X	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

# **Physical Dimensions**

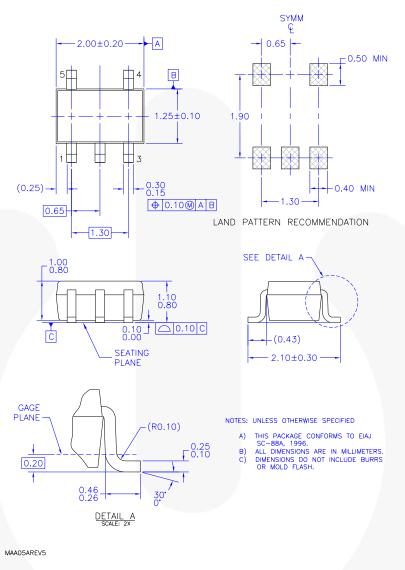


Figure 7. 5-Lead, SC70, EIAJ SC-88a, 1.25mm Wide

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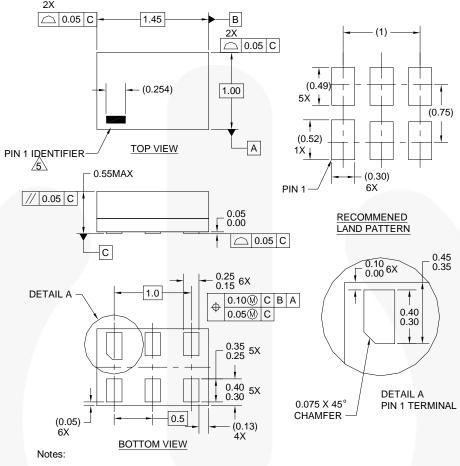
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Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
P5X	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

## **Physical Dimensions**



- 1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
- 2. DIMENSIONS ARE IN MILLIMETERS
- 3. DRAWING CONFORMS TO ASME Y14.5M-1994
- 4. FILENAME AND REVISION: MAC06AREV4
- 5 PIN ONE IDENTIFIER IS 2X LENGTH OF ANY

OTHER LINE IN THE MARK CODE LAYOUT.

Figure 8. 6-Lead, MicroPak™, 1.0mm Wide

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## **Tape and Reel Specifications**

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: http://www.fairchildsemi.com/products/logic/pdf/micropak\_tr.pdf.

Package Designator	Tape Section	<b>Cavity Number</b>	Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
L6X	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed





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