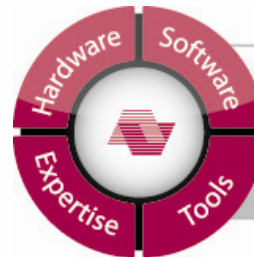


SILICA Xynergy Board

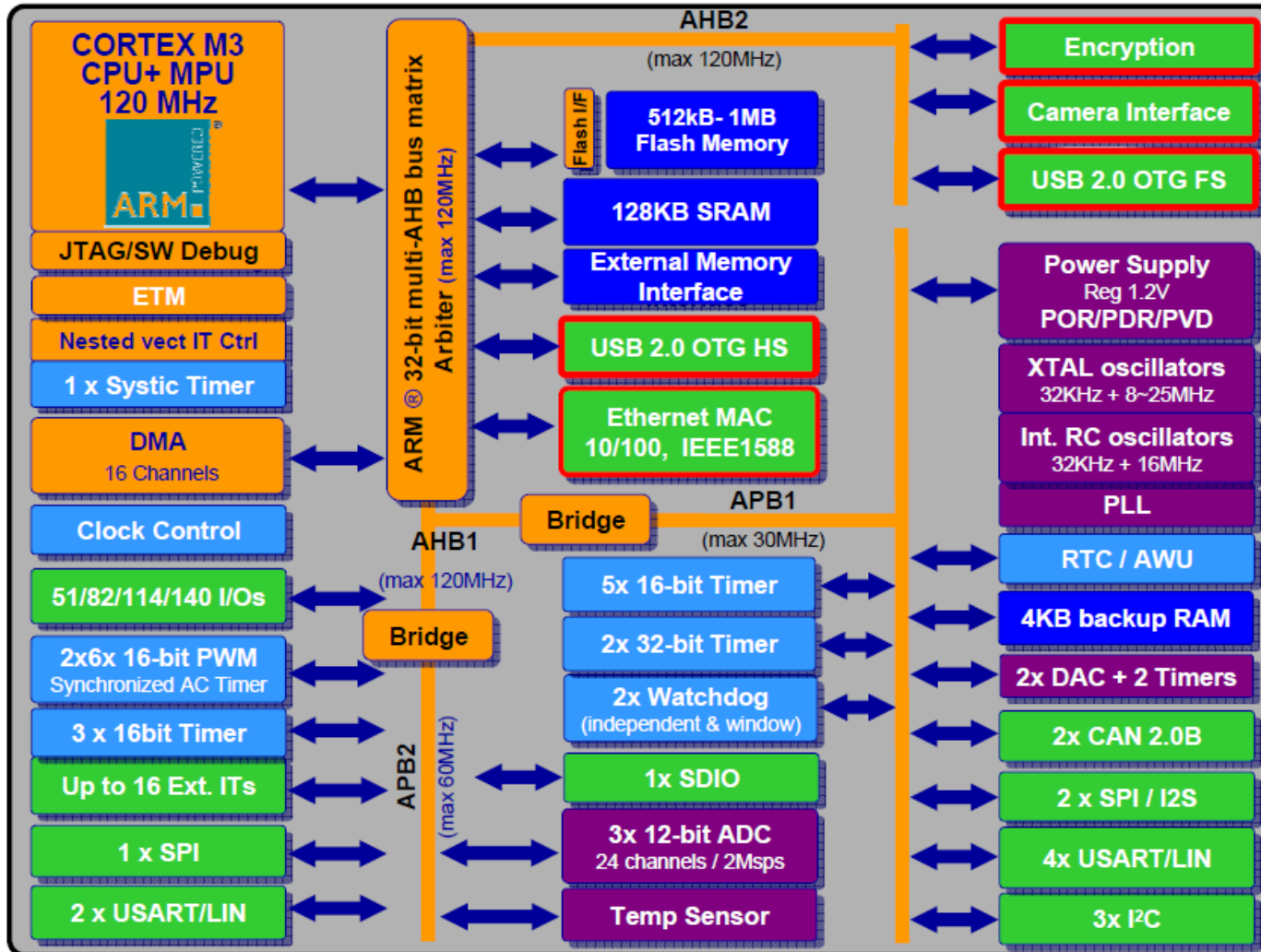
Explore the Synergies:
STM32 meets Spartan-6



Core 'n More

SILICA Microcontroller Solutions

Block Diagram / Features STM32F217





Cortex-M3 core's maximum processing performance with 0-wait state execution from Flash up to 120MHz

- ▶ **150 DMips at 120MHz**
- ▶ **Adaptive Real Time (ART memory acceleratorTM)**
 - ✚ 128-bits wide Flash with Prefetch
 - ✚ Intelligent Branch management
- ▶ **32-bit 7 layers AHB bus matrix interconnects**



188 μ A/MHz, 22.5mA at 120MHz

- ✚ ST's 90nm process, 1.2V core
- ✚ ST ART AcceleratorTM reducing accesses to Flash
- ▶ **Advanced low-power modes and features**
 - ✚ Backup SRAM and RTC
 - ✚ <1 μ A with RTC on
 - ✚ <1 μ A with 4-Kbyte backed up SRAM
 - ✚ <2 μ A with both on
- ▶ **VDD min down to 1.65V**



High Speed USB OTG

Audio PLL, I²S and USB synchronization

- ▶ Camera interface, 8- to 14-bit parallel, up to 48Mbyte/s at 48MHz
- ▶ Flexible static memory interface up to 60MHz
- ▶ Crypto/hash processor: 3DES, AES256/SHA-1, MD5, HMAC
- ▶ 3 SPIs running at up to 30Mbit/s,
- ▶ 6 USARTs running at up to 7.5Mbit/s
- ▶ 3x 12-bit ADC, 2 MSPS, up to 6MSPS in interleaved mode
- ▶ True random-number generator
- ▶ Fast GPIO (60 MHz toggling)



1-MByte Flash

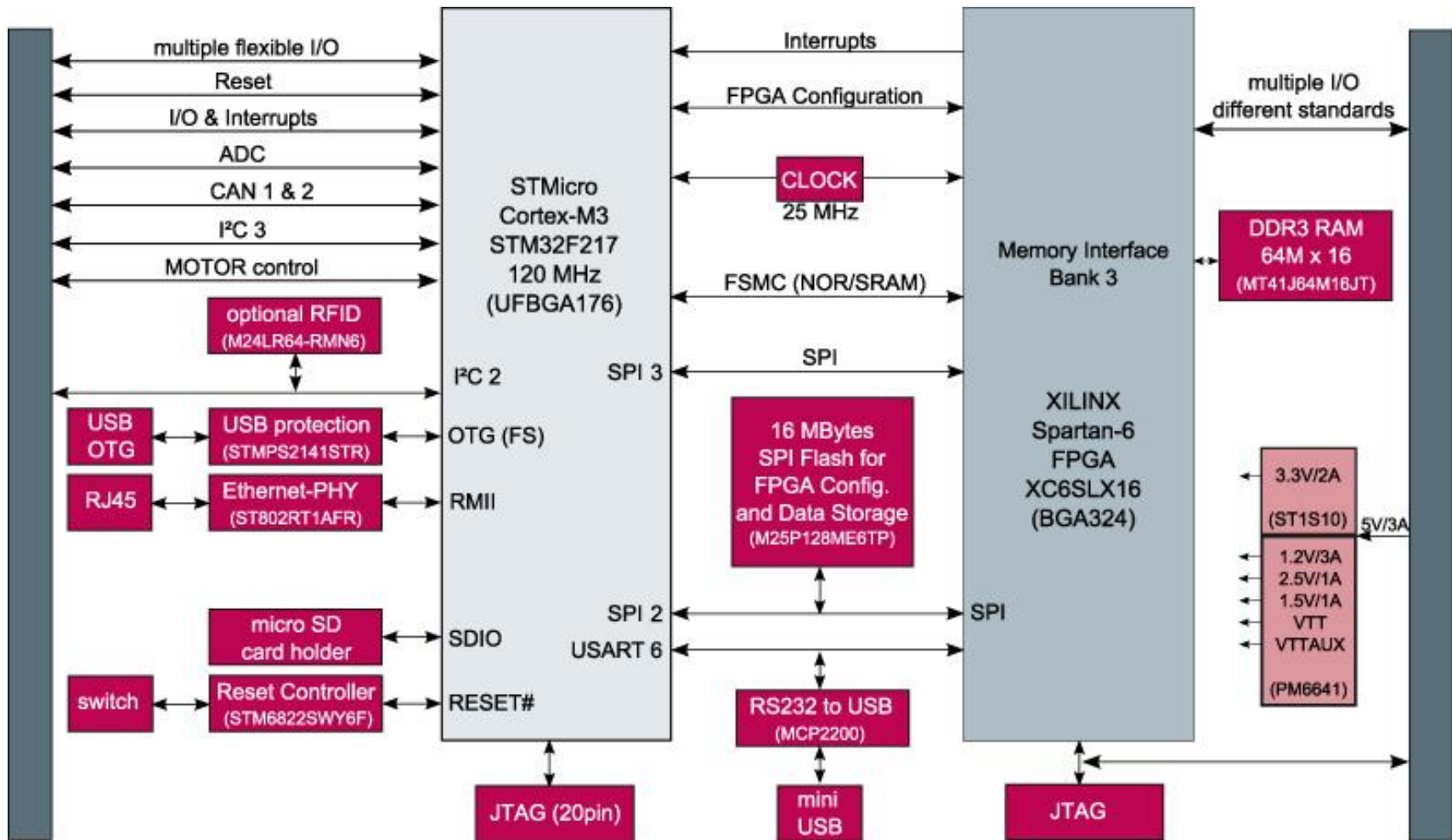
128-Kbyte SRAM

- ▶ 4-Kbytes back up SRAM: used as EEPROM to save application state, calibration data,
- ▶ 528 bytes of OTP memory to store critical user data such as Ethernet MAC addresses or cryptographic keys.

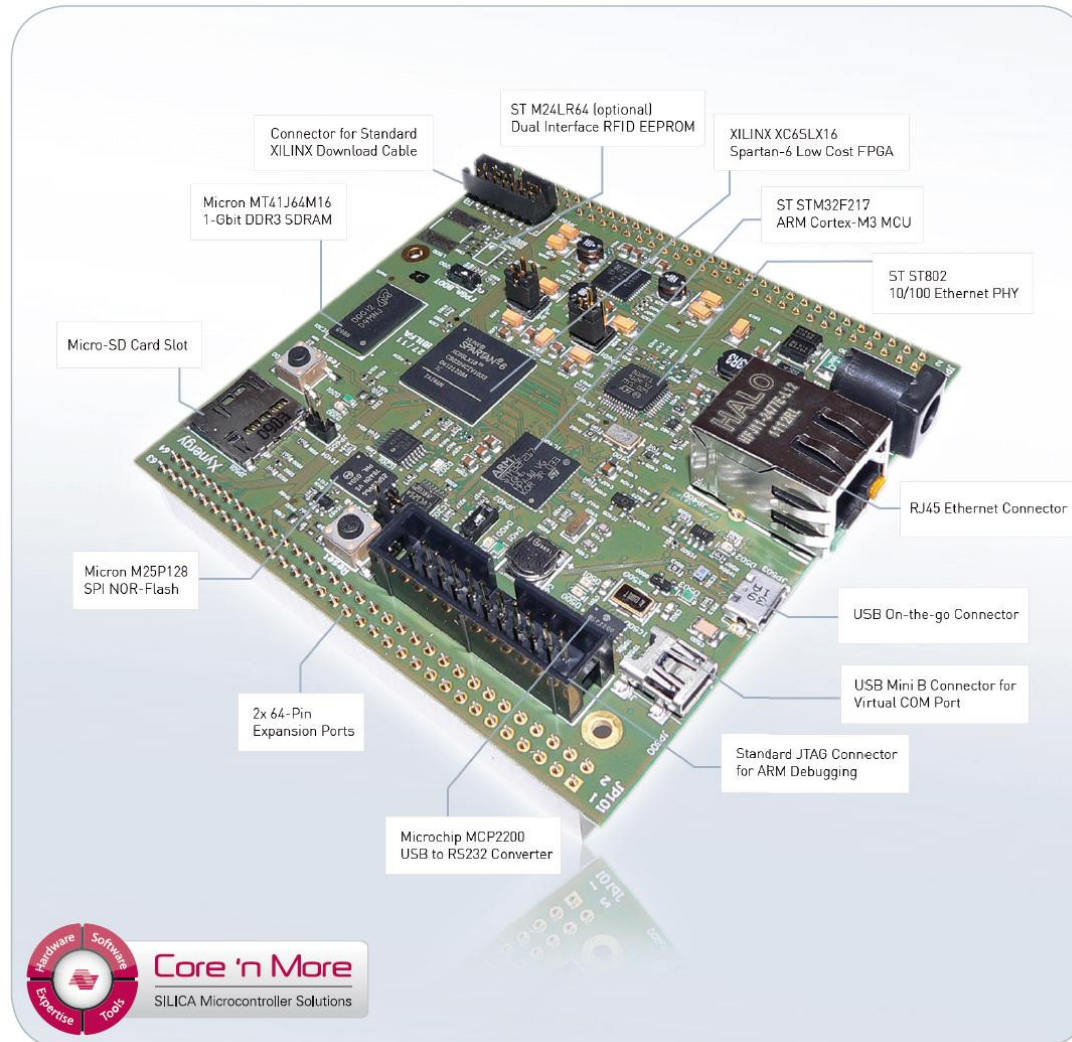
- ▶ **14.579** Logic Cells (6 Bit LUT, 2 Flip-Flops)
- ▶ **576Kb** Block RAM organized in **32** 18Kb Blocks
- ▶ **2** Clock Management Tiles (CMTs), each containing 2 DCMs and 1 PLL
- ▶ Maximum **232** Single-Ended or **116** Differential User I/Os
- ▶ **32** DSP48A1 Slices: Multiply Accumulate (MAC) and many more arithmetic functions
- ▶ **2** DDR2 / DDR3 SDRAM Memory Controller Block

XILINX.
SPARTAN 

SILICA Xynergy Board Block Diagram



Board Features



- 🌐 **Implementation of Industrial Ethernet IP in FPGA**
- 🌐 **Motorcontrol with FPGA acceleration of closed loop algorithms**
- 🌐 **General purpose Industrial Applications using Ethernet / USB / CAN / SPI / I²C**
- 🌐 **Access to DDR3 Memory**
- 🌐 **General Purpose Pre- and Coprocessing with FPGA , i.e. Digital Filtering ,
Advanced Crypto, Video etc.**
- 🌐 **Custom Interfaces**
- 🌐 **Evaluation of mixed Microcontroller / FPGA Designs**

- Development Tools available from Keil, IAR, Hitex, Lauterbach, Atollic, Raisonance (GNU)
- Free Standard- , USB-, Graphics- and Motorcontrol Libraries available from STMicroelectronics
- Free and advanced TCP/IP Stacks available from CMX, Free RTOS, Interniche, Keil, Micrium, NexGen and lwIP as open source
- RTOSs available from CMX, FreeRTOS, IAR, Keil, Micrium, Segger
- In-Circuit Debugger available from ST, Keil, IAR, Hitex, Lauterbach



